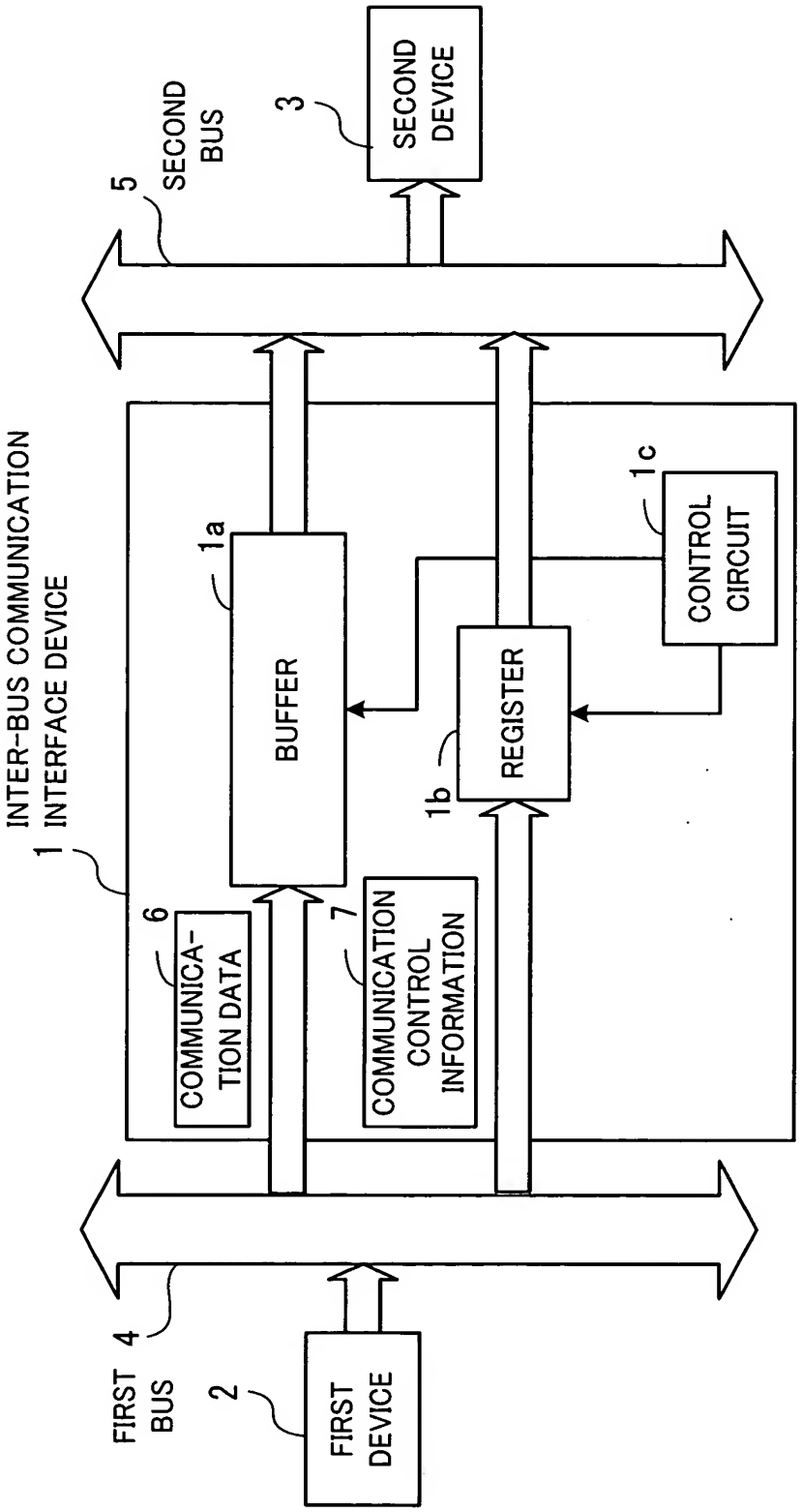

INTER-BUS COMMUNICATION INTERFACE DEVICE
1
BUFFER
1a
REGISTER
1b
CONTROL CIRCUIT
1c
COMMUNICA-TION DATA
6
COMMUNICATION CONTROL INFORMATION
7
FIRST BUS
4
FIRST DEVICE
2
SECOND BUS
5
SECOND DEVICE
3

FIG. 1

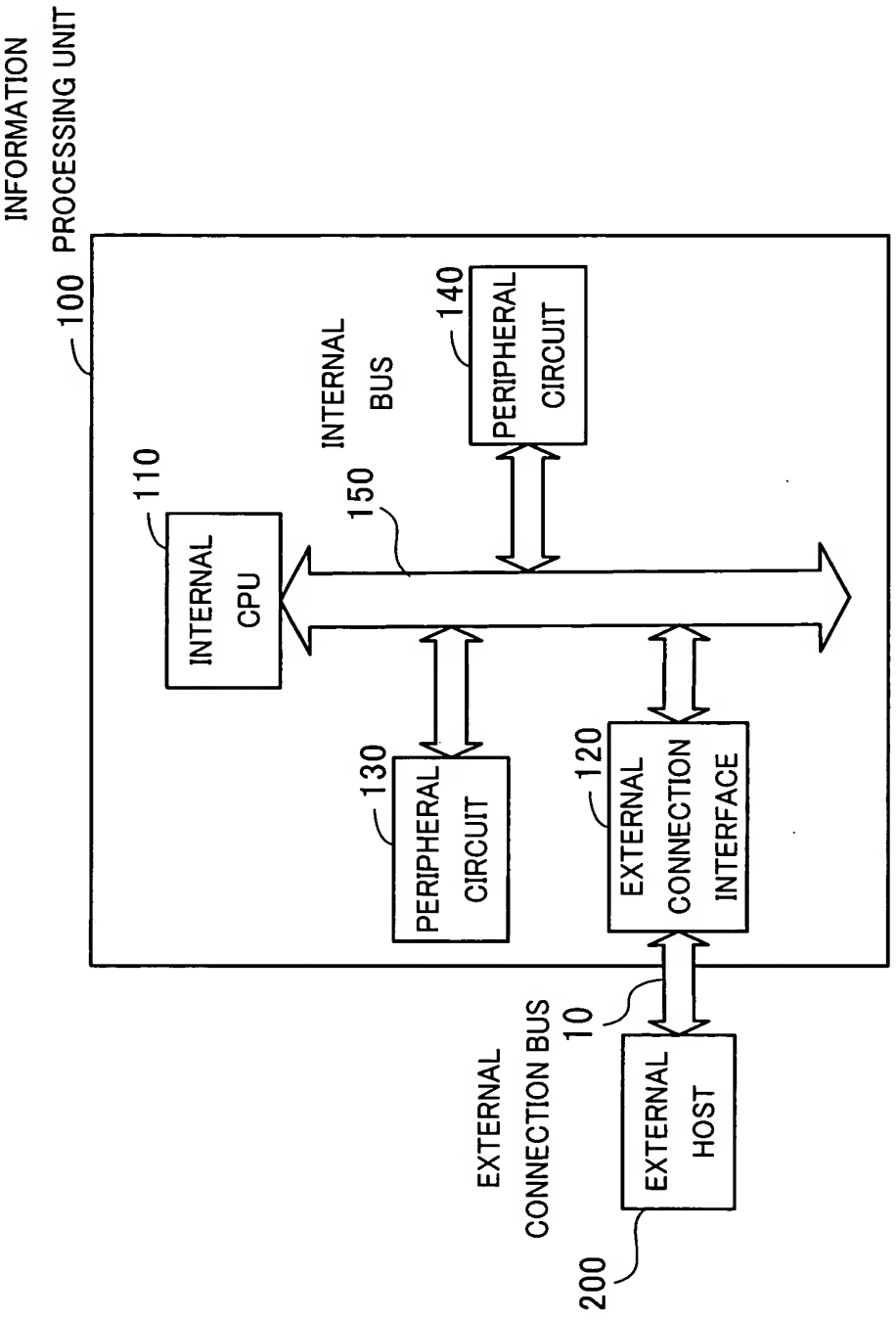

INFORMATION PROCESSING UNIT
100
INTERNAL CPU
110
INTERNAL BUS
150
PERIPHERAL CIRCUIT
140
PERIPHERAL CIRCUIT
130
EXTERNAL CONNECTION INTERFACE
120
EXTERNAL CONNECTION BUS
10
EXTERNAL HOST
200

FIG. 2

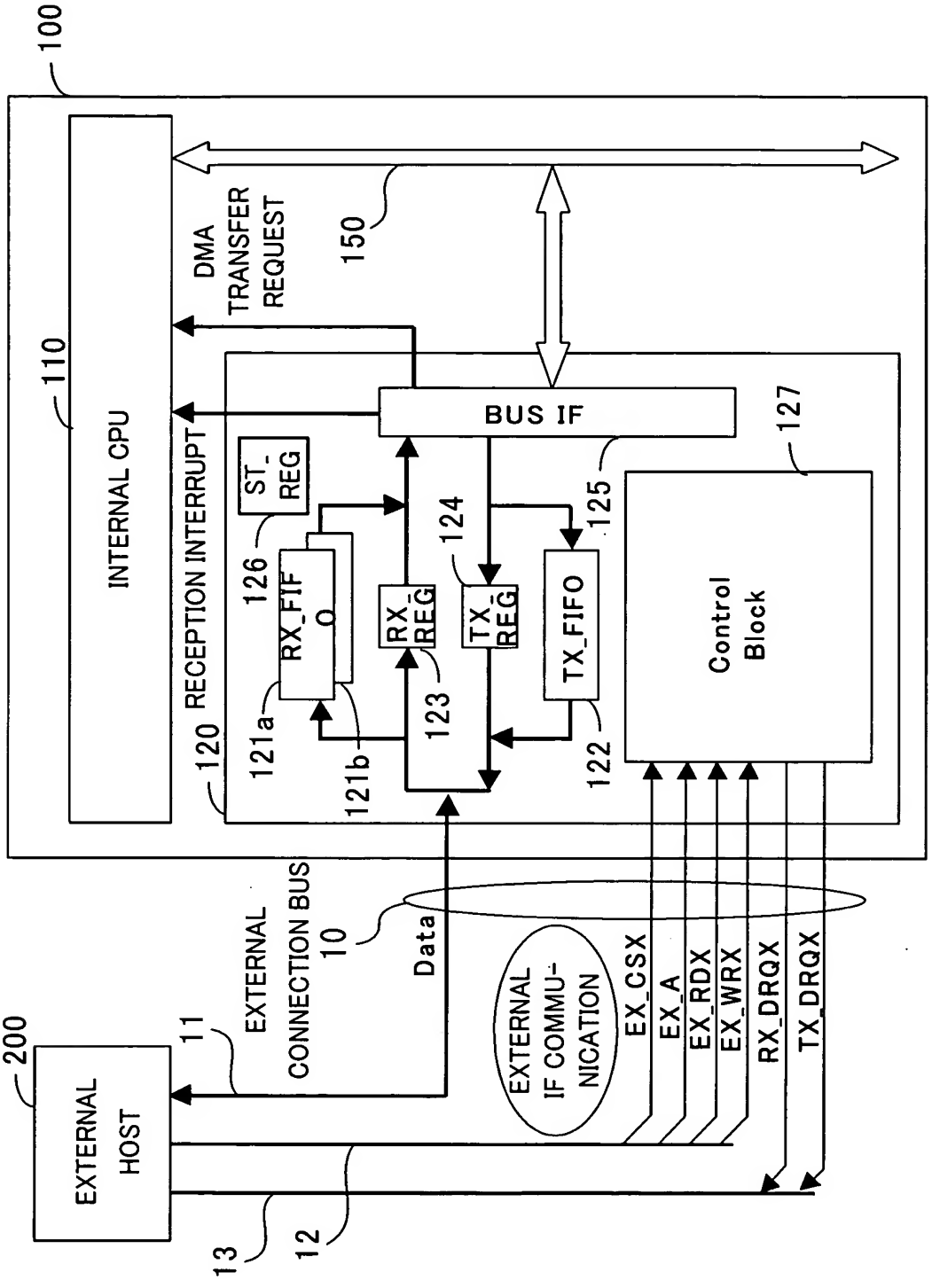

100
110
INTERNAL CPU
DMA TRANSFER REQUEST
150
RECEPTION INTERRUPT
120
BUS IF
127
ST_ REG
126
RX_FIF O
121a
121b
RX_ REG
123
TX_ REG
124
TX_FIFO
122
125
Control Block
EXTERNAL CONNECTION BUS
10
Data
EXTERNAL IF COMMU- NICATION
EX_CSX
EX_A
EX_RDX
EX_WRX
RX_DRQX
TX_DRQX
200
EXTERNAL HOST
11
13
12

FIG. 3

BIT	BIT NAME	INITIAL VALUE	R/W	FUNCTION
31:10	-	0	-	RESERVED
7:6	TX_FIFO	00	R	STATUS OF TX_FIFO INDICATE STATUS OF TX_FIFO 00 : NO DATA EXISTS IN TX_FIFO OR DATA HAS BEEN CLEARED 01 : DATA EXISTS IN TX_FIFO 10 : TX_FIFO IS FULL OF DATA 11 : RESERVED
5:4	RX_FIFO_B	00	R	STATUS OF RX_FIFO: SIDE-B INDICATES STATUS OF TWO-SIDED RX_FIFO (SIDE-A/SIDE-B) 00 : NO DATA EXISTS IN RX_FIFO (SIDE-B) OR DATA HAS BEEN CLEARED 01 : DATA EXISTS IN RX_FIFO (SIDE-B) 10 : RX_FIFO (SIDE-B) IS FULL OF DATA 11 : RESERVED
3:2	RX_FIFO_A	00	R	STATUS OF RX_FIFO: SIDE-A INDICATES STATUS OF TWO-SIDED RX_FIFO (SIDE-A/SIDE-B) 00 : NO DATA EXISTS IN RX_FIFO (SIDE-A) OR DATA HAS BEEN CLEARED 01 : DATA EXISTS IN RX_FIFO (SIDE-A) 10 : RX_FIFO (SIDE-A) IS FULL OF DATA 11 : RESERVED
⋮	⋮	⋮	⋮	⋮

FIG. 4

BIT	BIT NAME	INITIAL VALUES	R/W	FUNCTION
⋮	⋮	⋮	⋮	⋮
1	TX_REG_OUT	0	R	TX_REG REGISTER OUTPUT STATUS INDICATES DATA OUTPUT STATUS OF TX_REG REGISTER ※READ-CLEARING 0 : NO DATA OUTPUT FROM TX_REG REGISTER OR DATA HAS BEEN CLEARED 1 : DATA IS OUTPUT FROM TX_REG REGISTER
0	RX_REG_IN	0	R	RX_REG REGISTER INPUT STATUS INDICATES DATA INPUT STATUS OF RX_REG REGISTER ※READ-CLEARING 0 : NO DATA INPUT TO RX_REG REGISTER OR DATA HAS BEEN CLEARED 1 : DATA IS INPUT TO RX_REG REGISTER

FIG. 5

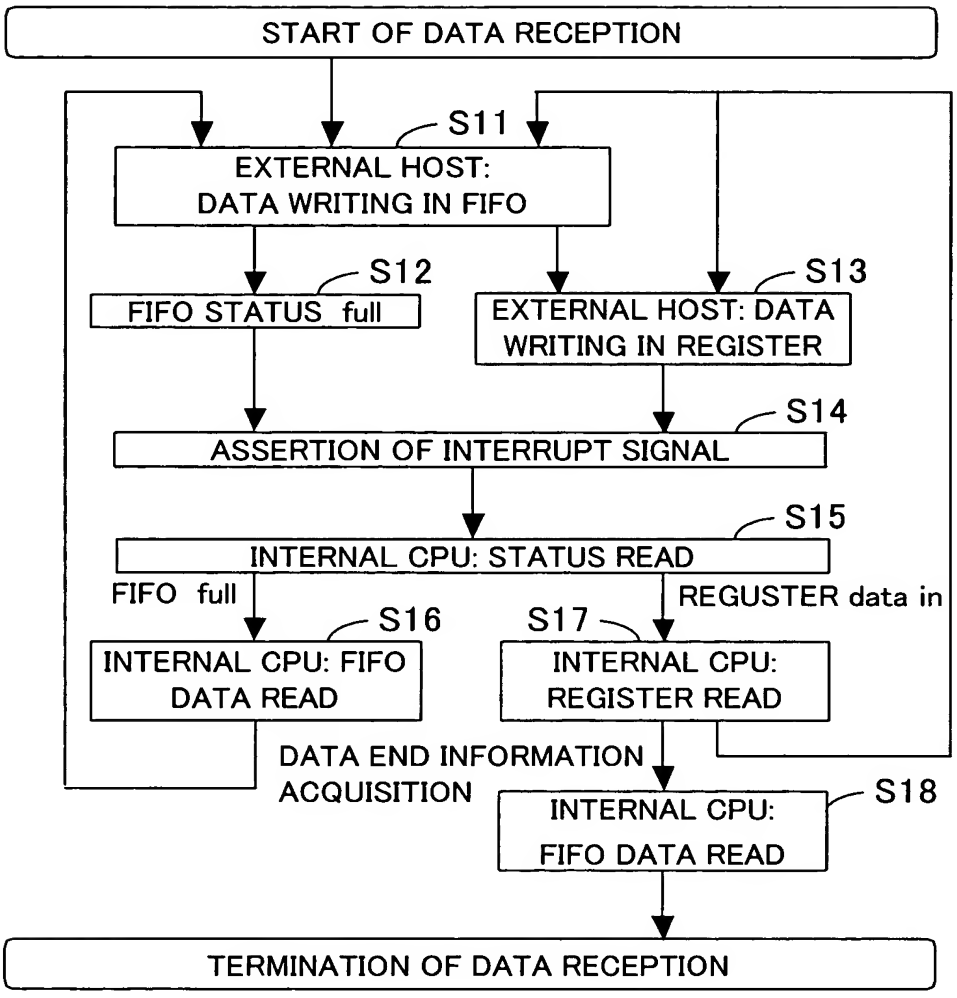

START OF DATA RECEPTION
S11
EXTERNAL HOST: DATA WRITING IN FIFO
S12
FIFO STATUS full
S13
EXTERNAL HOST: DATA WRITING IN REGISTER
S14
ASSERTION OF INTERRUPT SIGNAL
S15
INTERNAL CPU: STATUS READ
FIFO full
REGUSTER data in
S16
INTERNAL CPU: FIFO DATA READ
S17
INTERNAL CPU: REGISTER READ
DATA END INFORMATION ACQUISITION
S18
INTERNAL CPU: FIFO DATA READ
TERMINATION OF DATA RECEPTION

FIG. 6

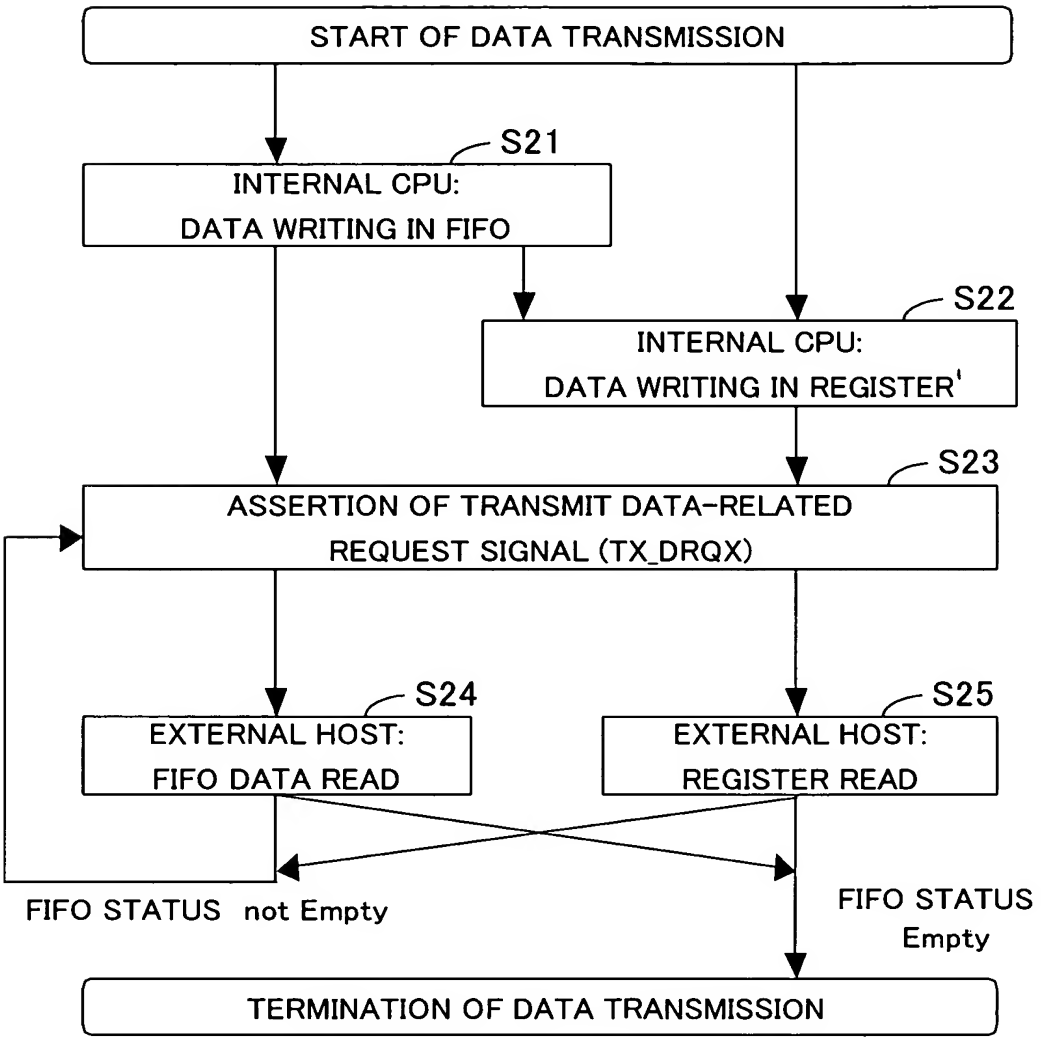

START OF DATA TRANSMISSION
S21
INTERNAL CPU:
DATA WRITING IN FIFO
S22
INTERNAL CPU:
DATA WRITING IN REGISTER'
S23
ASSERTION OF TRANSMIT DATA-RELATED
REQUEST SIGNAL (TX_DRQX)
S24
EXTERNAL HOST:
FIFO DATA READ
S25
EXTERNAL HOST:
REGISTER READ
FIFO STATUS not Empty
FIFO STATUS
Empty
TERMINATION OF DATA TRANSMISSION

FIG. 7

EXAMPLE OF CONFIGULATION OF SIGNALS VIA INTERNAL BUS

TERMINAL NAME	NAME	INPUT/ OUTPUT	FUNCTION
MCLKO	CLOCK SIGNAL	I	INPUT OF CLOCK SIGNAL
RSTXI	RESET SIGNAL	I	INPUT OF RESET SIGNAL
AO[3:0]	ADDRESS SIGNAL	I	INPUT OF ADDRESS SIGNAL
DO[31:0]	WRITE DATA SIGNAL	I	INPUT OF WRITE DATA
DI[31:0]	READ DATA SIGNAL	O	OUTPUT OF READ DATA
RDXO	READ STROBE SIGNAL	I	INPUT OF READ STROBE SIGNAL ACTIVE-LOW
WRXO[3:0]	WRITE STROBE SIGNAL	I	INPUT OF WRITE STROBE SIGNAL ACTIVE-LOW
CSX	CHIP SELECT SIGNAL	I	INPUT OF CHIP SELECT SIGNAL ACTIVE-LOW
INT	INTERRUPT SIGNAL	O	OUTPUT OF INTERRUPT SIGNAL ACTIVE-HIGH

FIG. 8

EXAMPLE OF CONFIGULATION OF SIGNALS VIA EXTERNAL TERMINAL

TERMINAL NAME	NAME	INPUT/ OUTPUT	FUNCTION
EX_DI[15:0]	INPUT DATA SIGNAL	I	INPUT OF DATA
EX_DO[15:0]	OUTPUT DATA SIGNAL	O	OUTPUT OF DATA
EX_DOE	DATA BUS DIRECTION SWITCHING SIGNAL	O	OUTPUT OF DATA BUS DIRECTION SWITCHING SIGNAL
EX_CSX	CHIP SELECT SIGNAL	I	INPUT OF CHIP SELECT SIGNAL ACTIVE-LOW
EX_A	ADDRESS SIGNAL	I	INPUT OF ADDRESS SIGNAL " 0" FOR REGISTER SELECTION AND " 1" FOR FIFO SELECTION
EX_RDX	READ STROBE SIGNAL	I	INPUT OF READ STROBE SIGNAL ACTIVE-LOW
EX_WRX	WRITE STROBE SIGNAL	I	INPUT OF WRITE STROBE SIGNAL ACTIVE-LOW
RX_DRQX	RECEIVE DATA-RELATED REQUEST SIGNAL	O	OUTPUT OF RECEIVE DATA-RELATED REQUEST SIGNAL ACTIVE-LOW ASSERTED " LOW" UNTIL RECEIVE FIFO BECOMES FULL
TX_DRQX	TRANSMIT DATA-RELATED REQUEST SIGNAL	O	OUTPUT OF TRANSMIT DATA-RELATED REQUEST SIGNAL ACTIVE-LOW ASSERTTED " LOW" WHEN READABLE DATA EXISTS IN TRANSMIT REGISER OR TRANSMIT INTENAL RAM

FIG. 9

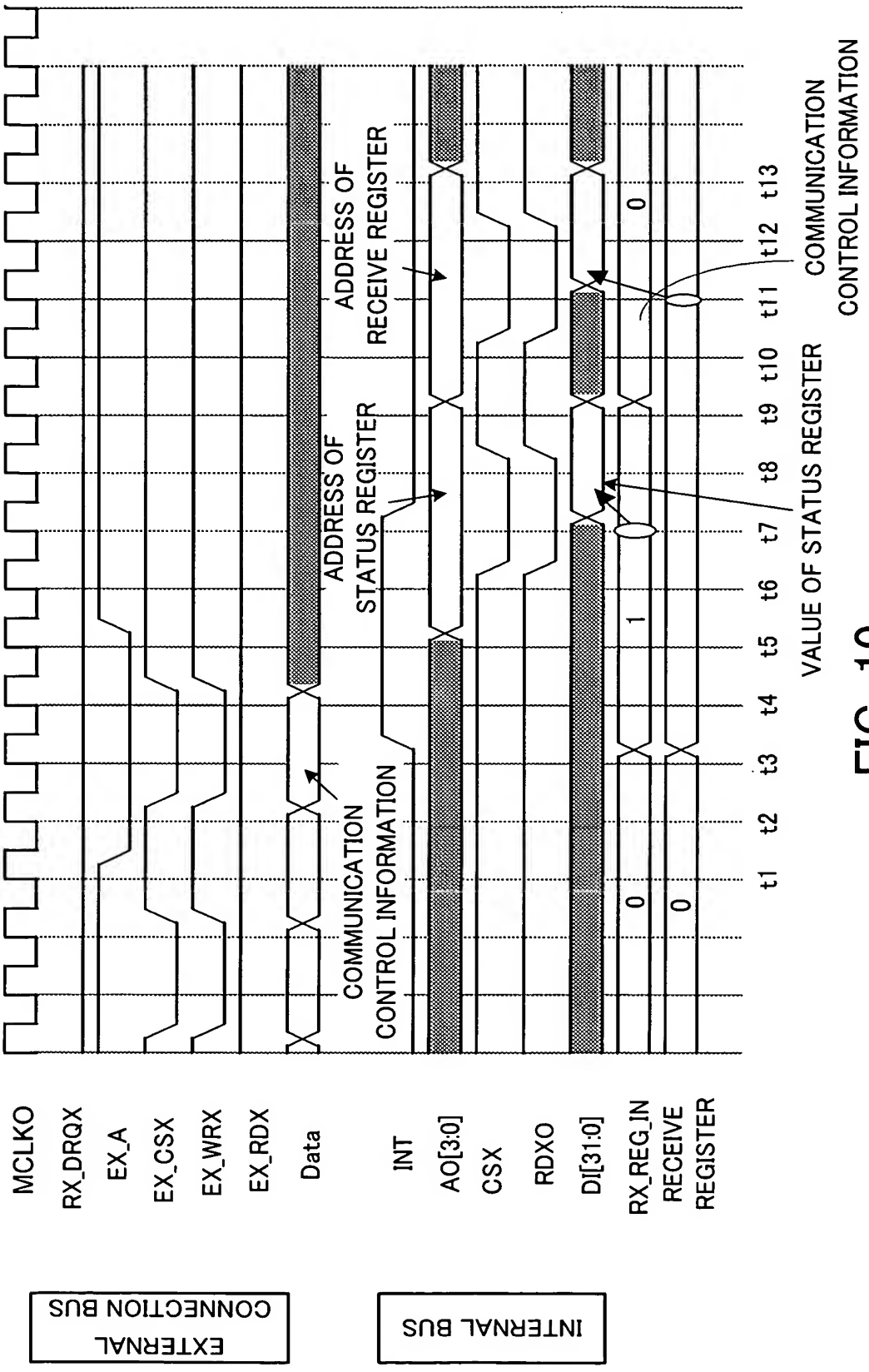

EXTERNAL CONNECTION BUS
INTERNAL BUS
MCLKO
RX_DRQX
EX_A
EX_CSX
EX_WRX
EX_RDX
Data
INT
AO[3:0]
CSX
RDXO
DI[31:0]
RX_REG_IN
RECEIVE REGISTER
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
0
0
1
0
COMMUNICATION CONTROL INFORMATION
ADDRESS OF STATUS REGISTER
ADDRESS OF RECEIVE REGISTER
VALUE OF STATUS REGISTER
COMMUNICATION CONTROL INFORMATION

FIG. 10

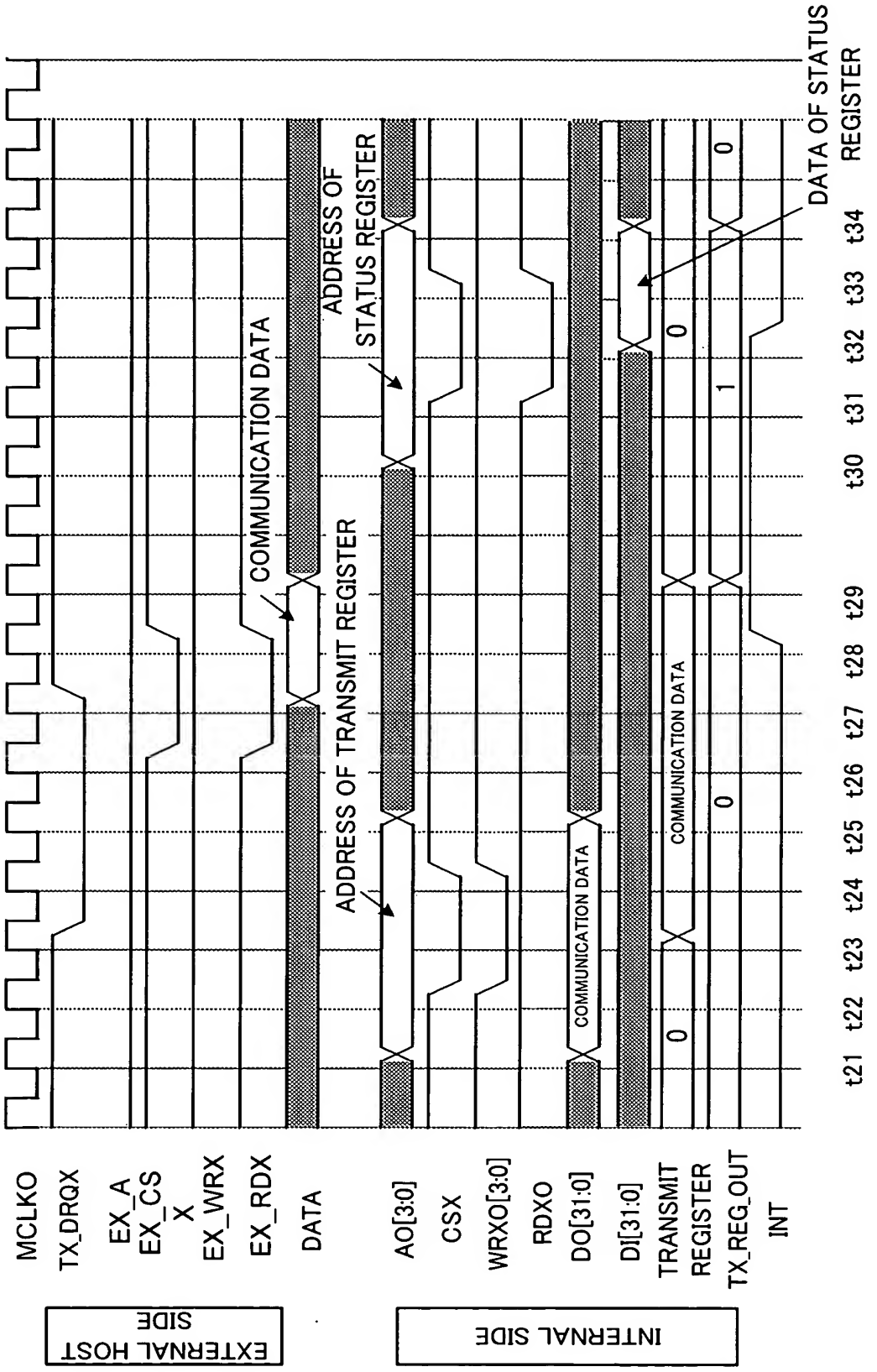

EXTERNAL HOST SIDE
INTERNAL SIDE
MCLKO
TX_DRQX
EX_A
EX_CS
X
EX_WRX
EX_RDX
DATA
AO[3:0]
CSX
WRXO[3:0]
RDXO
DO[31:0]
DI[31:0]
TRANSMIT REGISTER
TX_REG_OUT
INT
COMMUNICATION DATA
ADDRESS OF TRANSMIT REGISTER
COMMUNICATION DATA
ADDRESS OF STATUS REGISTER
DATA OF STATUS REGISTER
t21 t22 t23 t24 t25 t26 t27 t28 t29 t30 t31 t32 t33 t34
0
0
1
0
0

FIG. 11

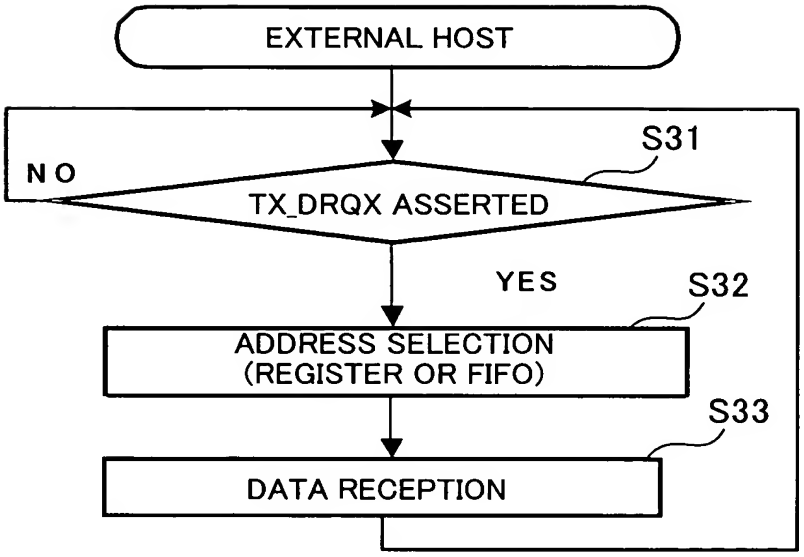

EXTERNAL HOST
S31
NO
TX_DRQX ASSERTED
YES
S32
ADDRESS SELECTION
(REGISTER OR FIFO)
S33
DATA RECEPTION

FIG. 12

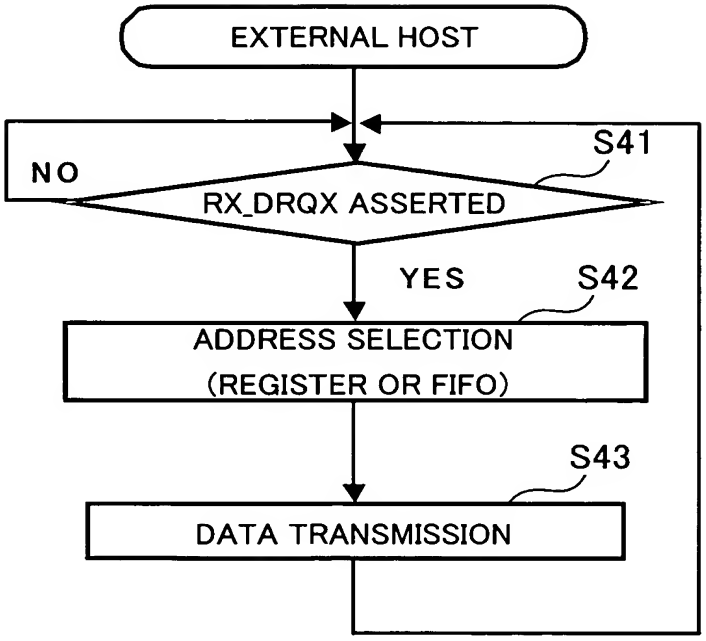

EXTERNAL HOST
S41
NO
RX_DRQX ASSERTED
YES
S42
ADDRESS SELECTION
(REGISTER OR FIFO)
S43
DATA TRANSMISSION

FIG. 13

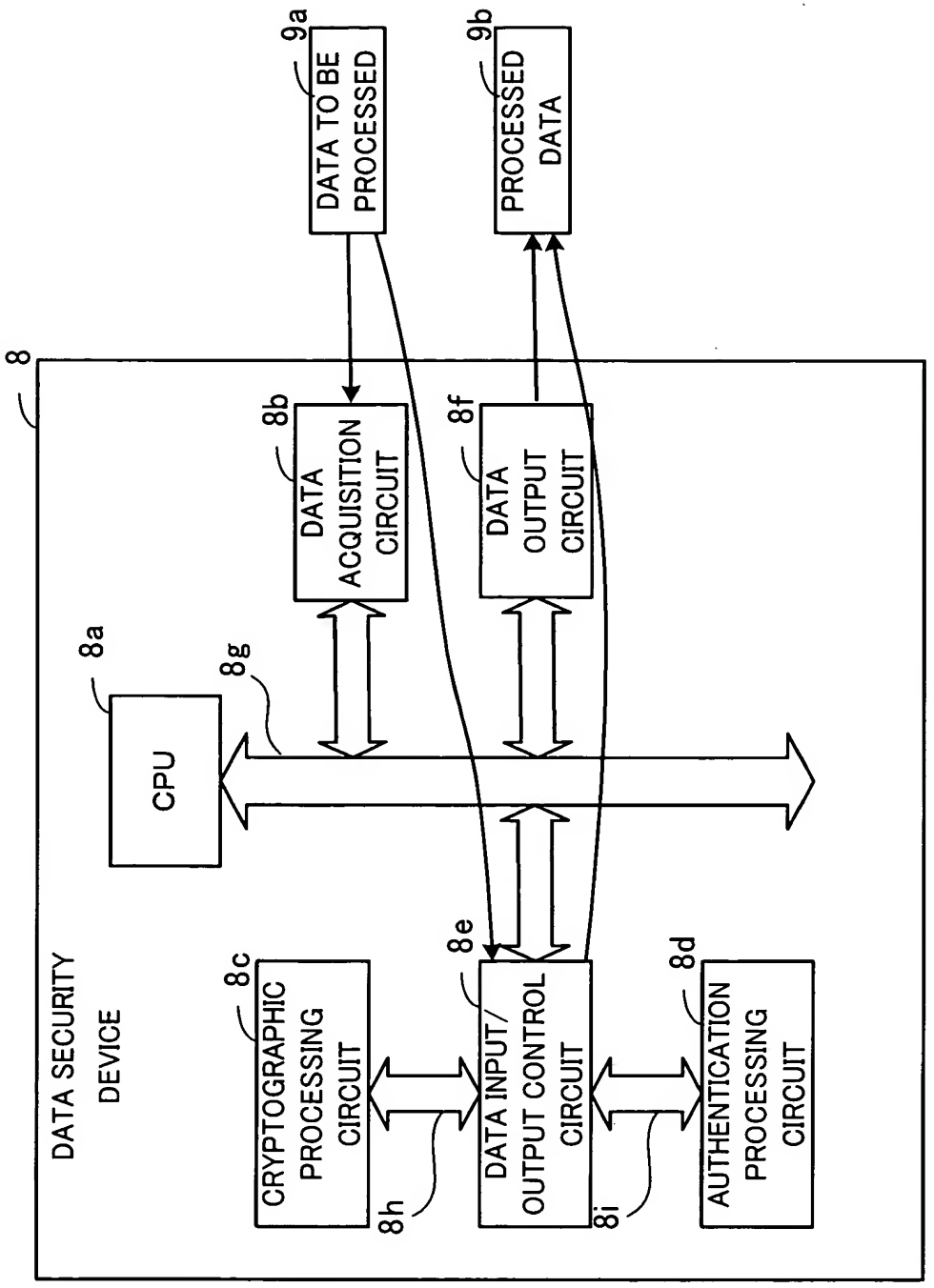

9a
DATA TO BE PROCESSED
9b
PROCESSED DATA
8
8b
DATA ACQUISITION CIRCUIT
8f
DATA OUTPUT CIRCUIT
8a
CPU
8g
8e
8c
CRYPTOGRAPHIC PROCESSING CIRCUIT
DATA INPUT/ OUTPUT CONTROL CIRCUIT
8d
AUTHENTICATION PROCESSING CIRCUIT
DATA SECURITY DEVICE
8h
8i

FIG. 14

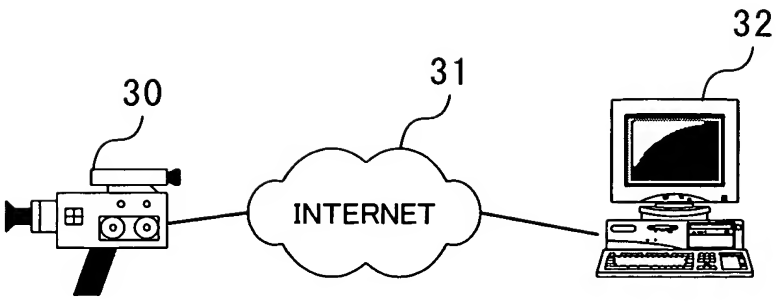


FIG. 15

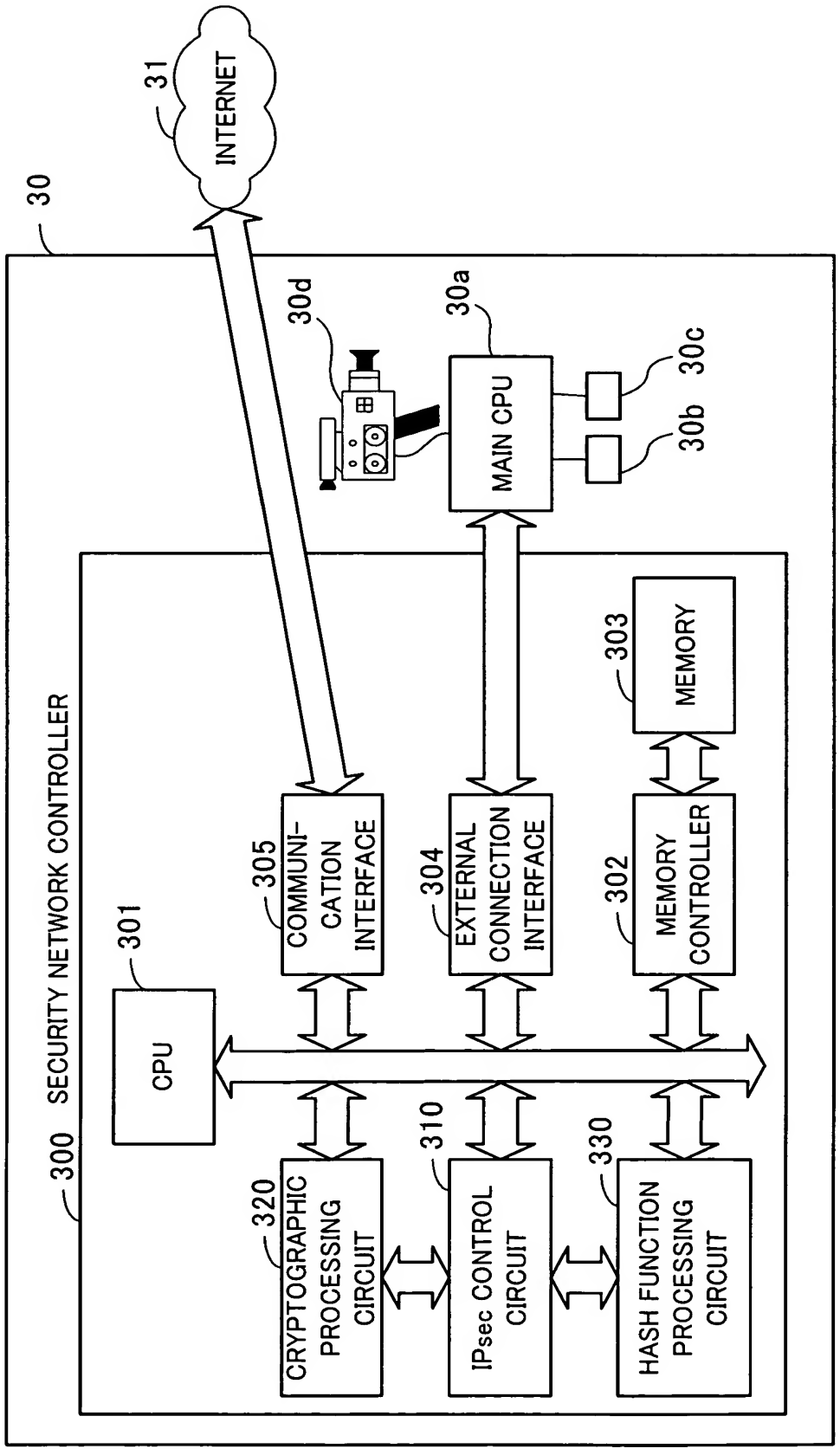

31
INTERNET
30
30d
30a
30c
30b
MAIN CPU
SECURITY NETWORK CONTROLLER
300
301
CPU
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
303
MEMORY
302
MEMORY CONTROLLER
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 16

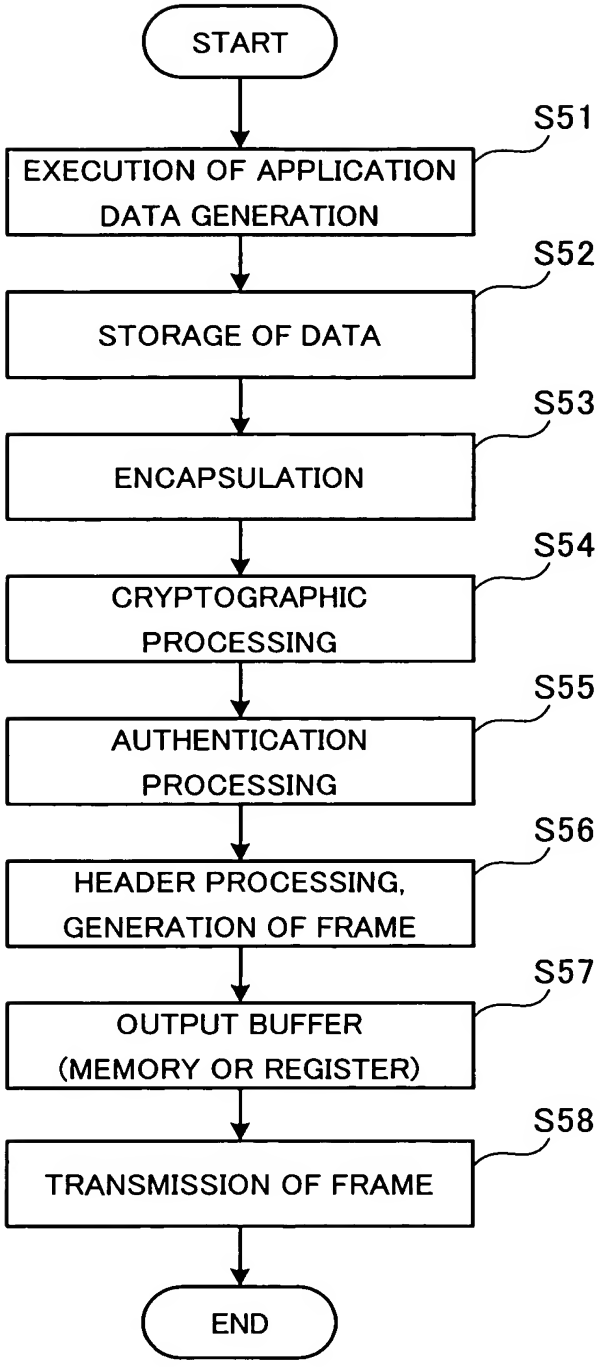

START
S51
EXECUTION OF APPLICATION DATA GENERATION
S52
STORAGE OF DATA
S53
ENCAPSULATION
S54
CRYPTOGRAPHIC PROCESSING
S55
AUTHENTICATION PROCESSING
S56
HEADER PROCESSING, GENERATION OF FRAME
S57
OUTPUT BUFFER (MEMORY OR REGISTER)
S58
TRANSMISSION OF FRAME
END

FIG. 17

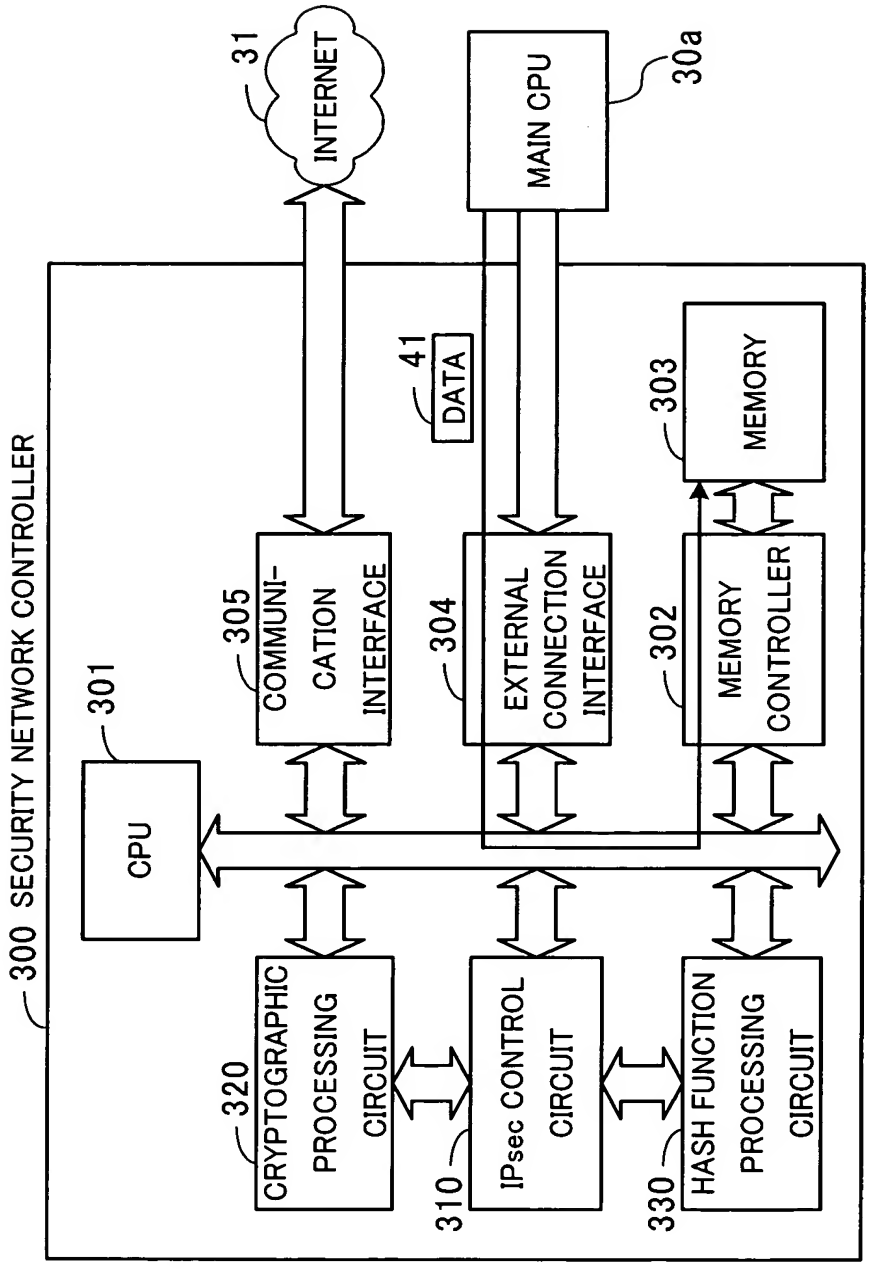

300 SECURITY NETWORK CONTROLLER
31
INTERNET
MAIN CPU
30a
41
DATA
303
MEMORY
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
302
MEMORY CONTROLLER
301
CPU
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 18

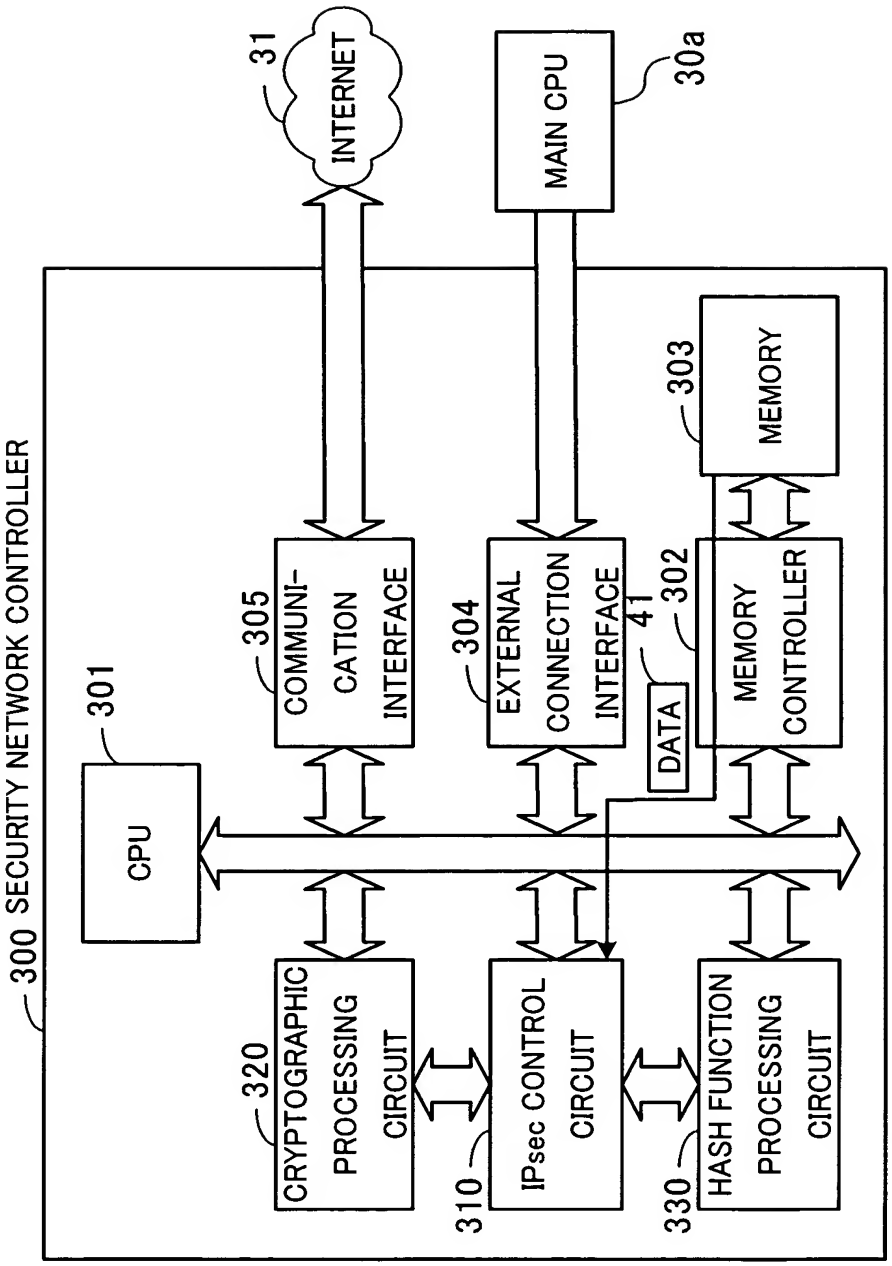

300 SECURITY NETWORK CONTROLLER
31
INTERNET
MAIN CPU
30a
303
MEMORY
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
41
DATA
302
MEMORY CONTROLLER
301
CPU
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 19

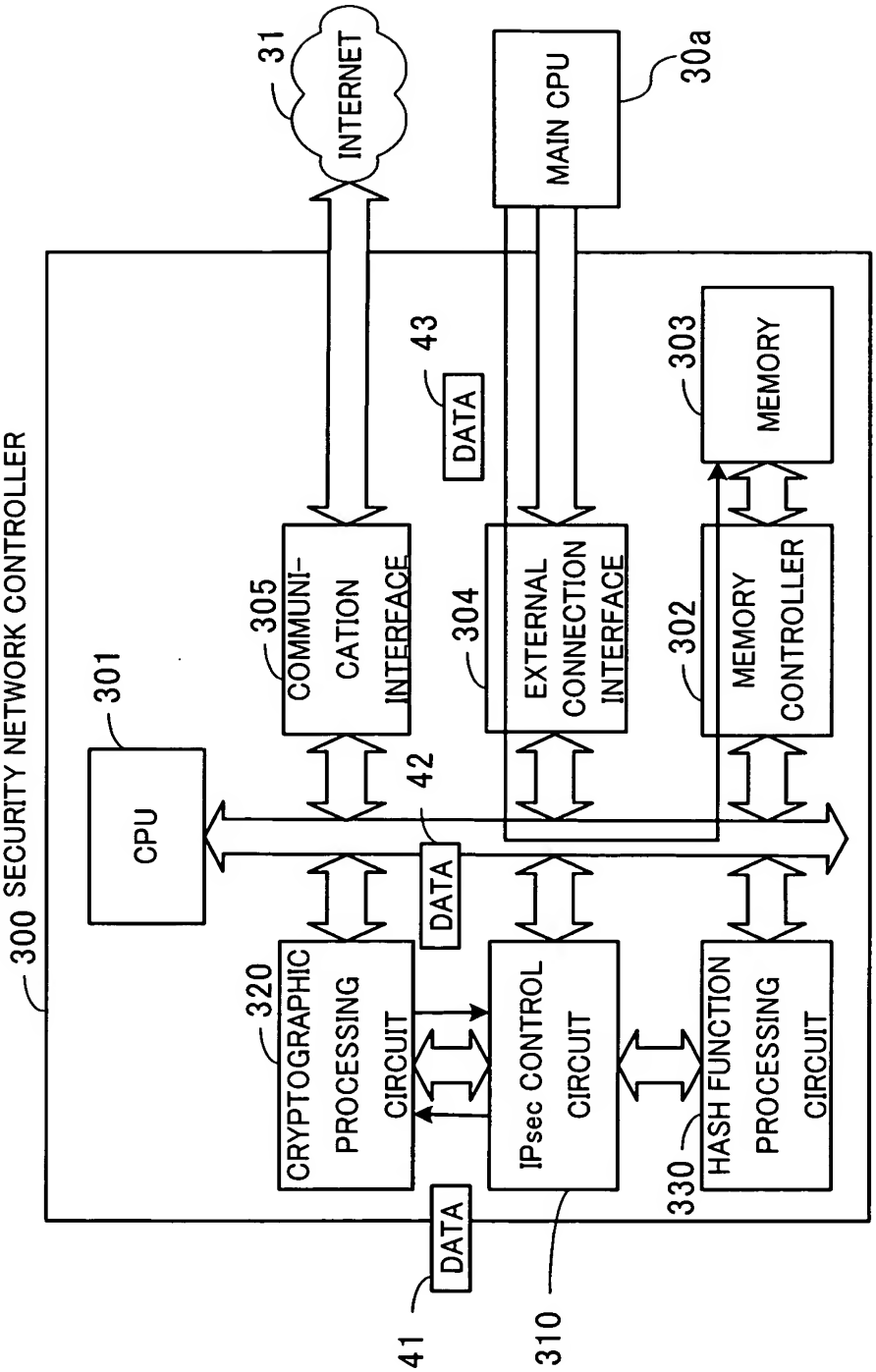

31
INTERNET
MAIN CPU
30a
43
DATA
303
MEMORY
300 SECURITY NETWORK CONTROLLER
305
COMMUNI-
CATION
INTERFACE
304
EXTERNAL
CONNECTION
INTERFACE
302
MEMORY
CONTROLLER
301
CPU
42
DATA
320
CRYPTOGRAPHIC
PROCESSING
CIRCUIT
IPsec CONTROL
CIRCUIT
HASH FUNCTION
PROCESSING
CIRCUIT
330
DATA
41
310

FIG. 20

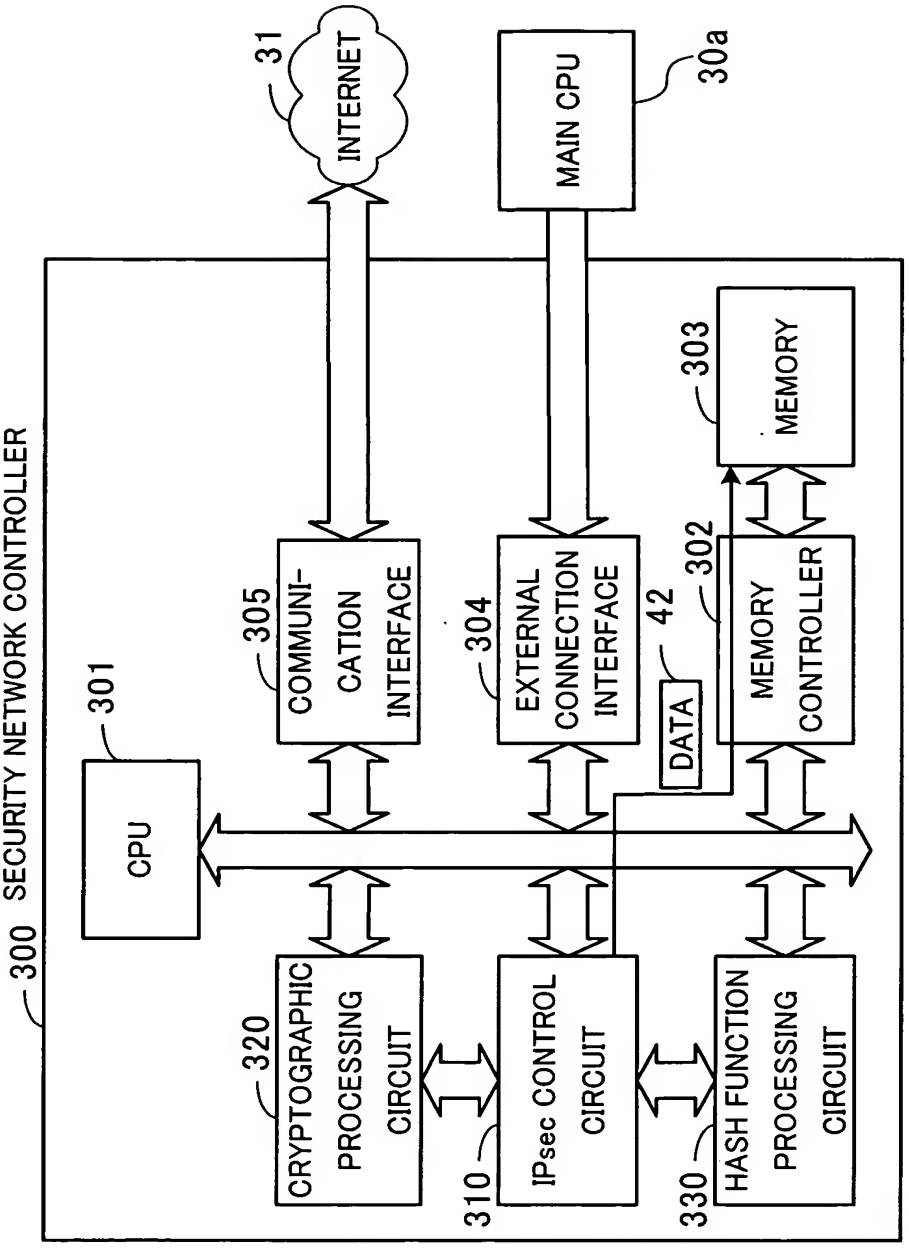

300 SECURITY NETWORK CONTROLLER
31
INTERNET
MAIN CPU
30a
303
MEMORY
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
302
MEMORY CONTROLLER
42
DATA
301
CPU
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 21

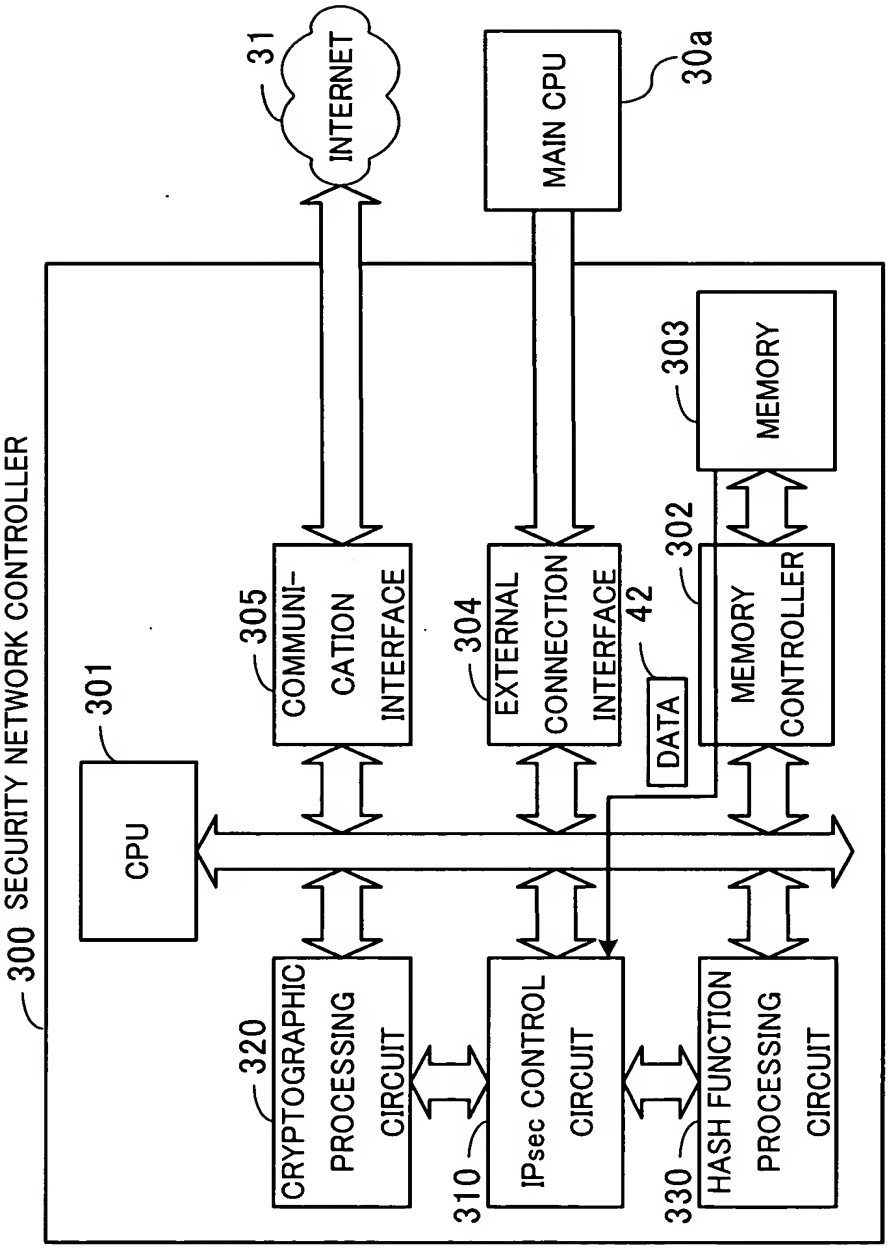

300 SECURITY NETWORK CONTROLLER
31
INTERNET
MAIN CPU
30a
303
MEMORY
302
MEMORY CONTROLLER
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
42
DATA
301
CPU
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 22

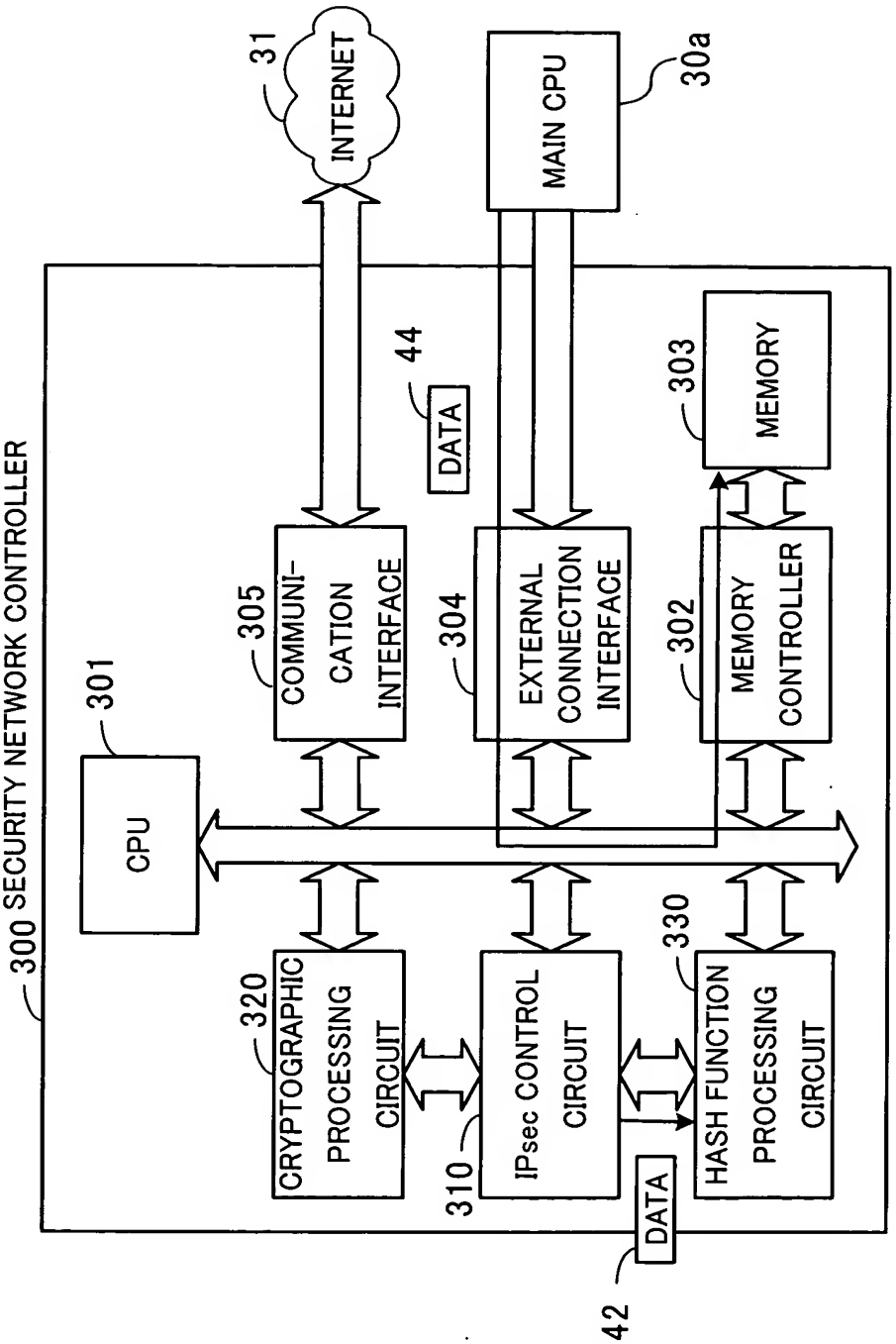

31
INTERNET
MAIN CPU
30a
300 SECURITY NETWORK CONTROLLER
44
DATA
303
MEMORY
305
COMMUNI-
CATION
INTERFACE
304
EXTERNAL
CONNECTION
INTERFACE
302
MEMORY
CONTROLLER
301
CPU
320
CRYPTOGRAPHIC
PROCESSING
CIRCUIT
310
IPsec CONTROL
CIRCUIT
330
HASH FUNCTION
PROCESSING
CIRCUIT
DATA
42

FIG. 23

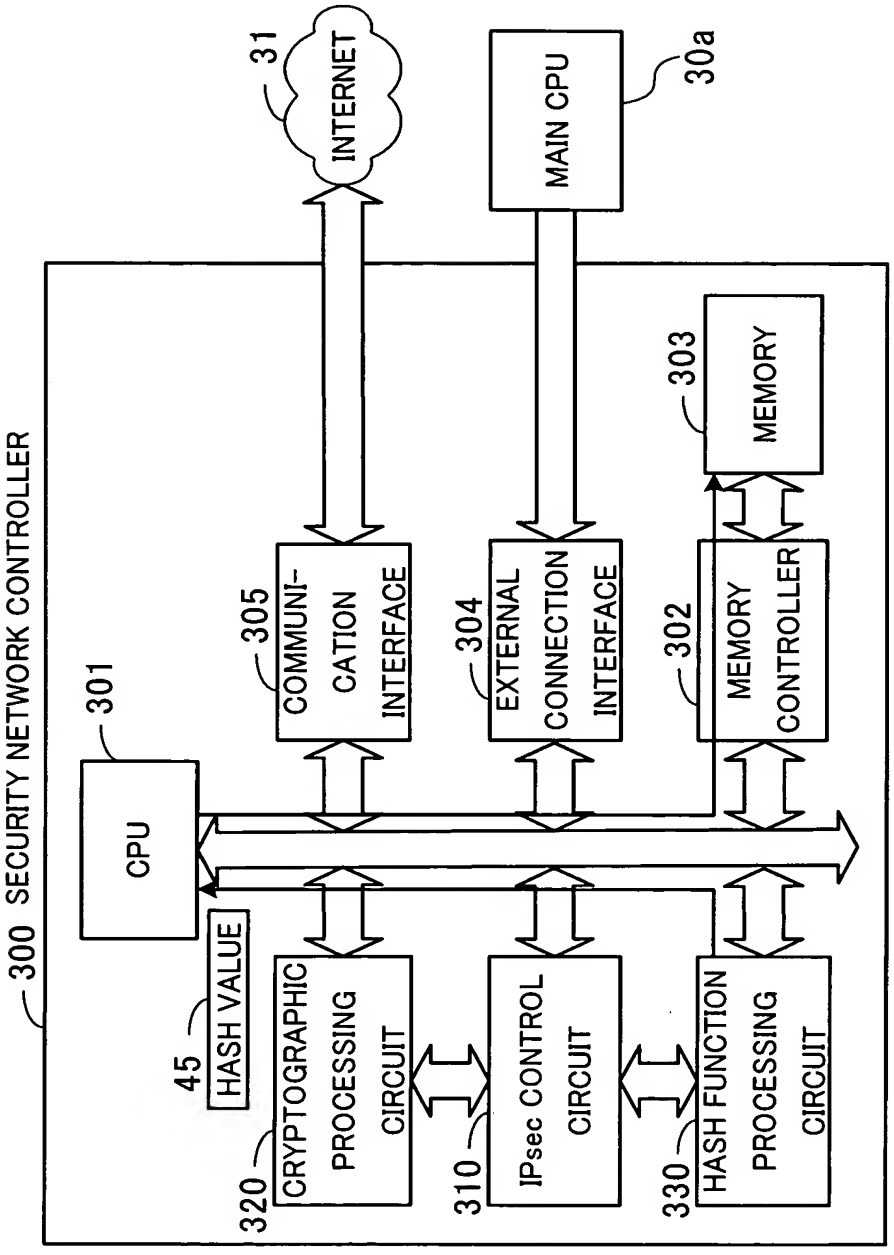

300 SECURITY NETWORK CONTROLLER
31
INTERNET
MAIN CPU
30a
303
MEMORY
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
302
MEMORY CONTROLLER
301
CPU
45
HASH VALUE
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 24

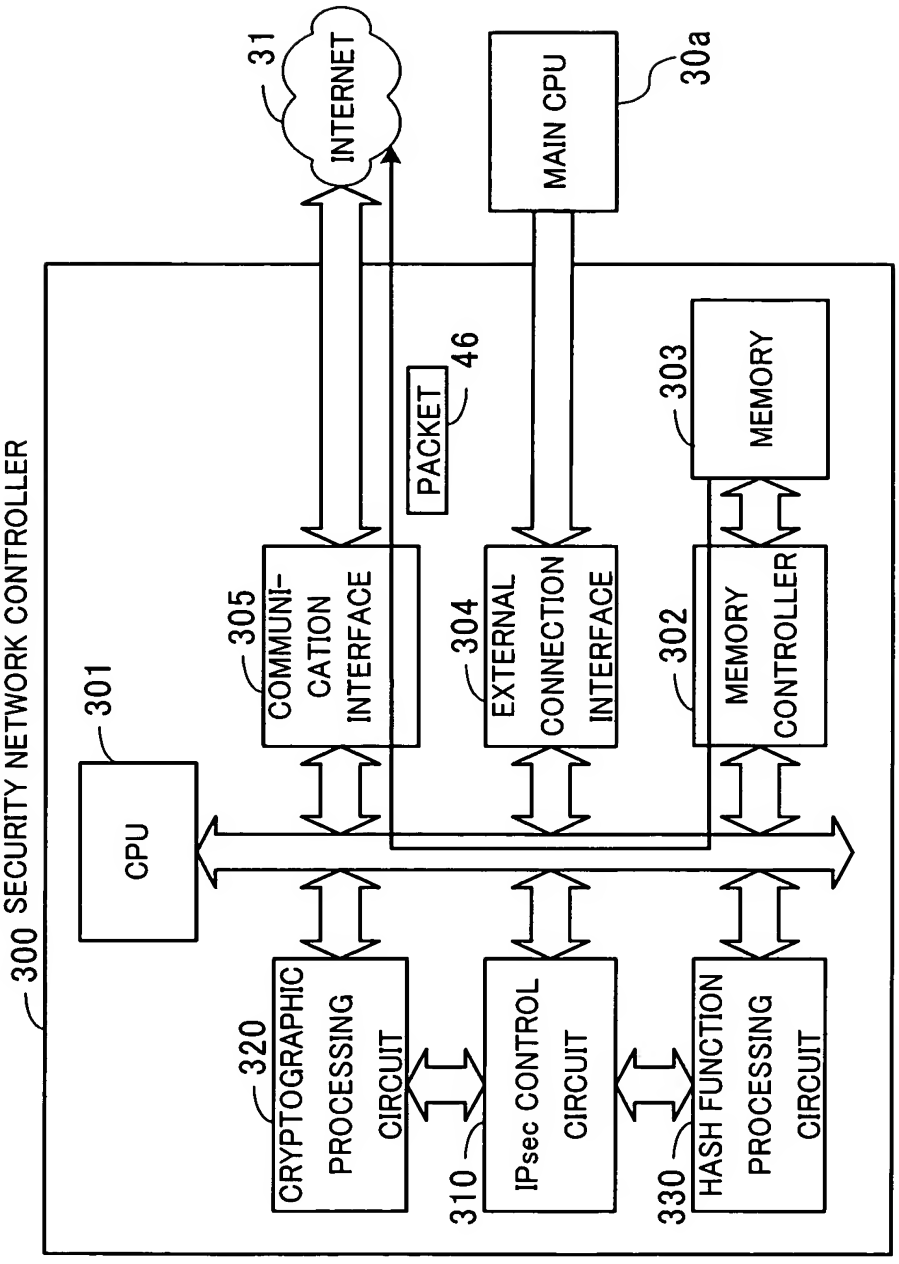

31
INTERNET
MAIN CPU
30a
300 SECURITY NETWORK CONTROLLER
PACKET
46
303
MEMORY
305
COMMUNI-CATION INTERFACE
304
EXTERNAL CONNECTION INTERFACE
302
MEMORY CONTROLLER
301
CPU
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
310
IPsec CONTROL CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 25

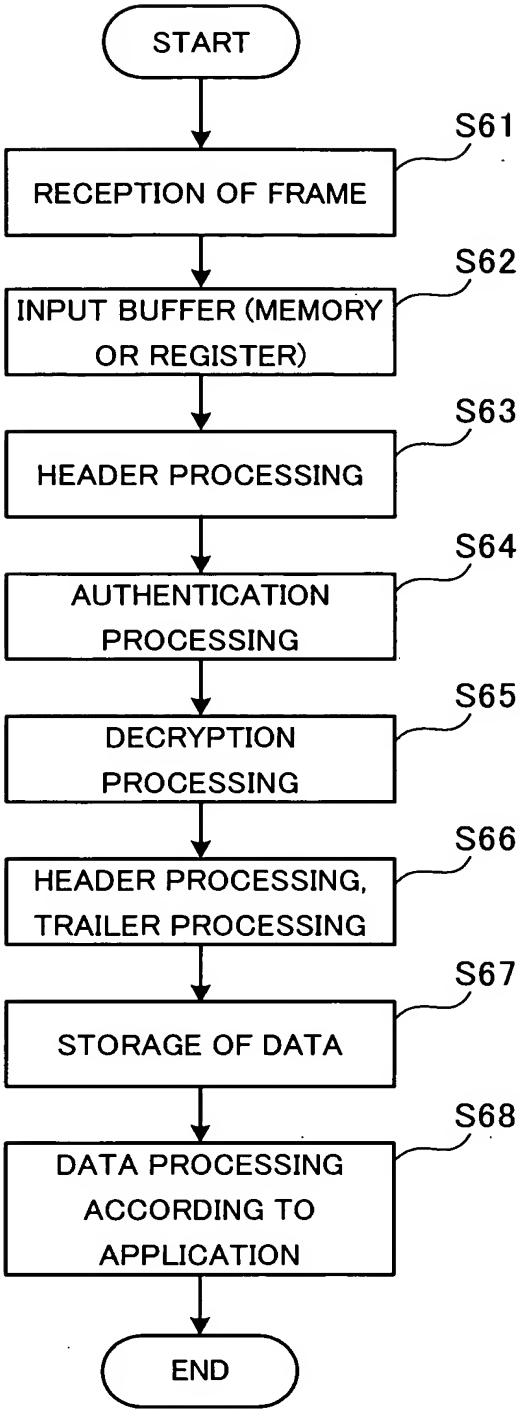

START
S61
RECEPTION OF FRAME
S62
INPUT BUFFER (MEMORY OR REGISTER)
S63
HEADER PROCESSING
S64
AUTHENTICATION PROCESSING
S65
DECRYPTION PROCESSING
S66
HEADER PROCESSING, TRAILER PROCESSING
S67
STORAGE OF DATA
S68
DATA PROCESSING ACCORDING TO APPLICATION
END

FIG. 26

Title: INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA SECURITY DEVICE
Inventor: Kenichi IIZUKA et al.
Docket Number: 108273-00006

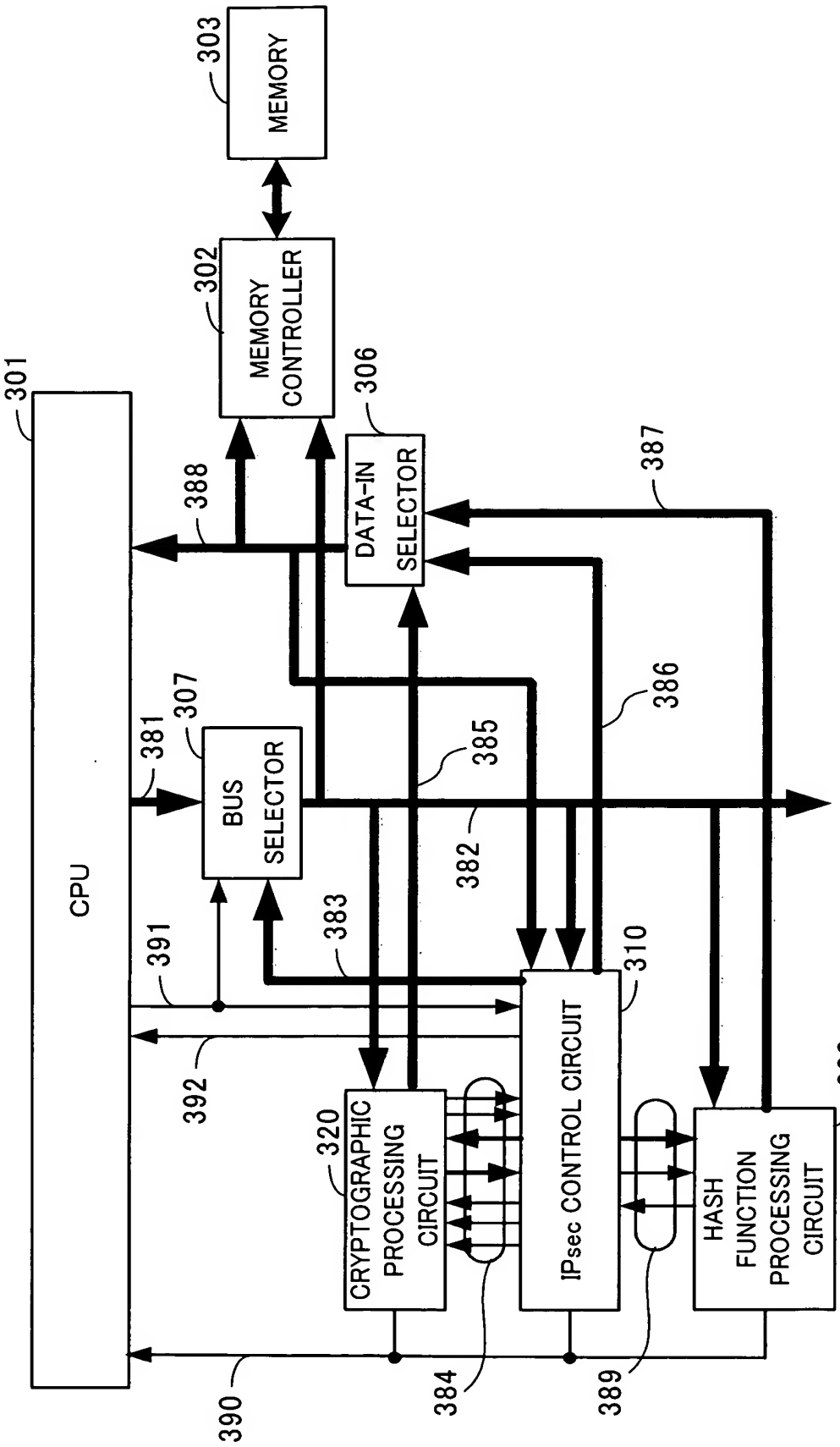


FIG. 27

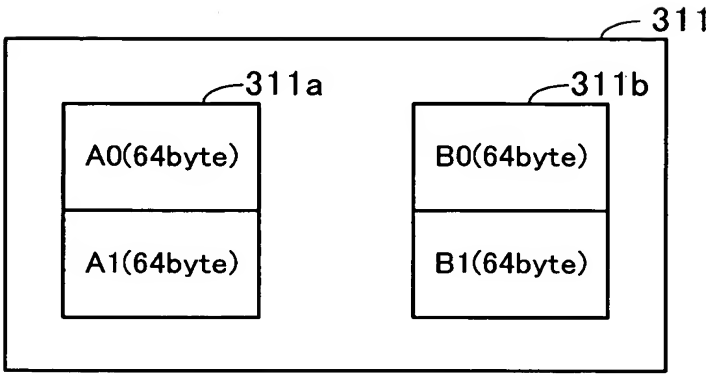


FIG. 28

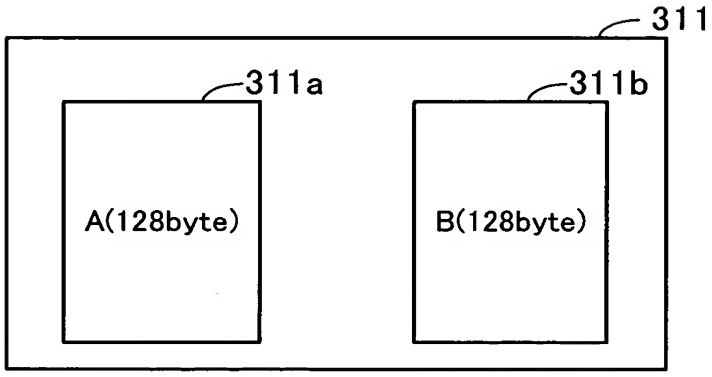


FIG. 29

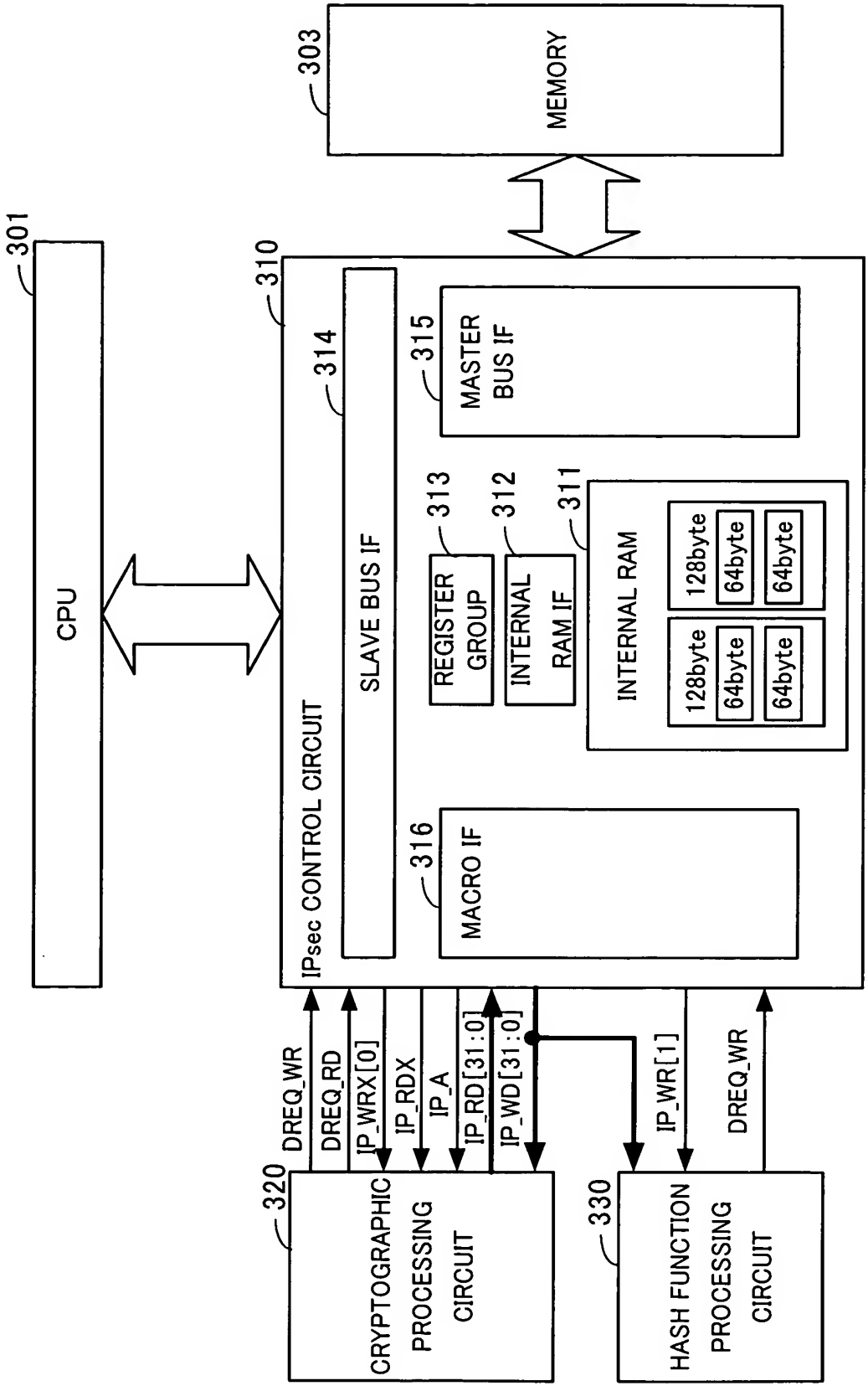

303
MEMORY
301
CPU
310
IPsec CONTROL CIRCUIT
314
SLAVE BUS IF
315
MASTER BUS IF
313
REGISTER GROUP
312
INTERNAL RAM IF
311
INTERNAL RAM
128byte
64byte
64byte
128byte
64byte
64byte
316
MACRO IF
DREQ_WR
DREQ_RD
IP_WRX[0]
IP_RDX
IP_A
IP_RD[31:0]
IP_WD[31:0]
IP_WR[1]
DREQ_WR
320
CRYPTOGRAPHIC PROCESSING CIRCUIT
330
HASH FUNCTION PROCESSING CIRCUIT

FIG. 30

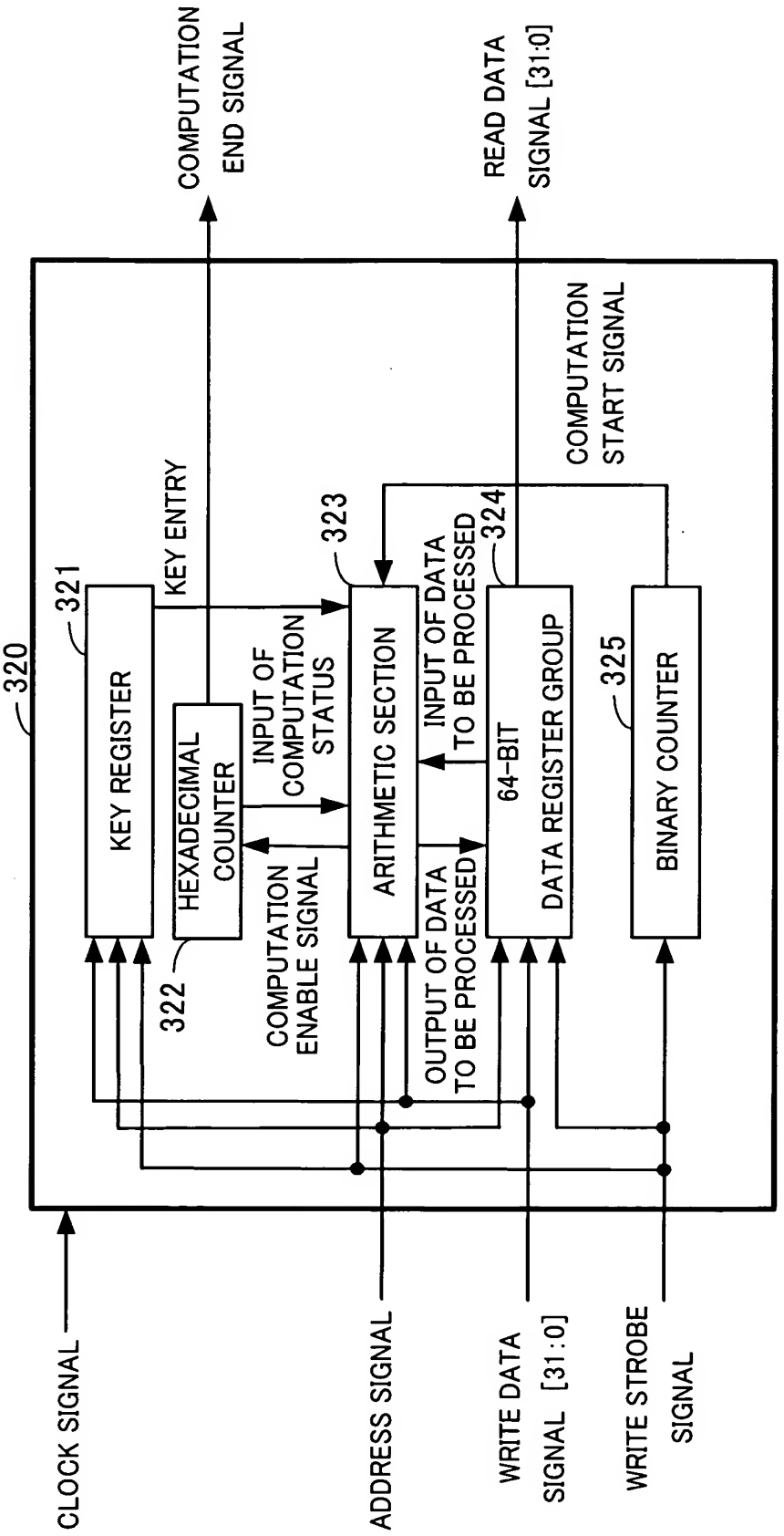

COMPUTATION END SIGNAL
READ DATA SIGNAL [31:0]
320
321
KEY REGISTER
KEY ENTRY
322
HEXADECIMAL COUNTER
INPUT OF COMPUTATION STATUS
COMPUTATION ENABLE SIGNAL
323
ARITHMETIC SECTION
INPUT OF DATA TO BE PROCESSED
OUTPUT OF DATA TO BE PROCESSED
324
64-BIT DATA REGISTER GROUP
COMPUTATION START SIGNAL
325
BINARY COUNTER
CLOCK SIGNAL
ADDRESS SIGNAL
WRITE DATA SIGNAL [31:0]
WRITE STROBE SIGNAL

FIG. 31

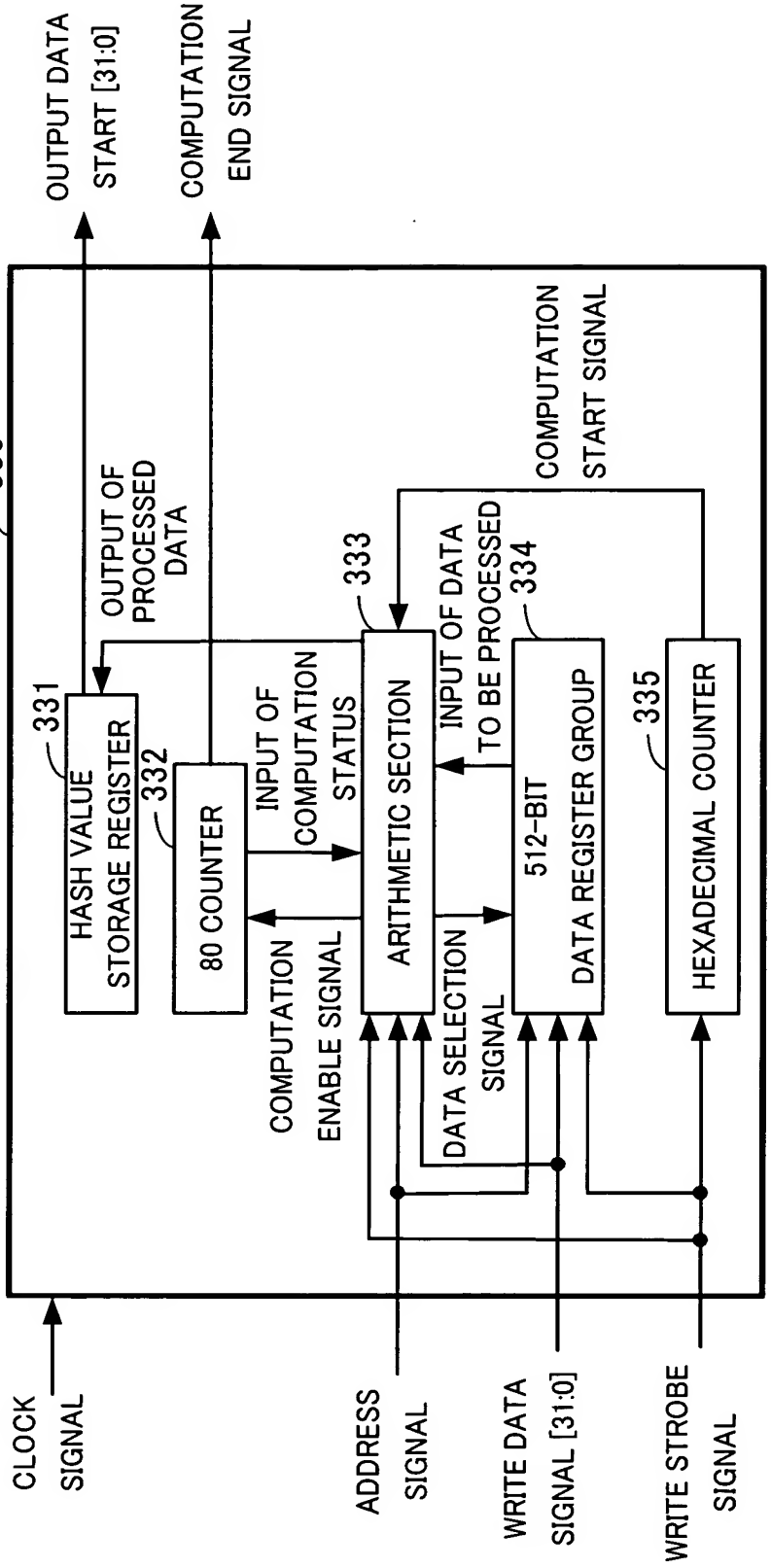

OUTPUT DATA START [31:0]
COMPUTATION END SIGNAL
330
OUTPUT OF PROCESSED DATA
COMPUTATION START SIGNAL
331
HASH VALUE STORAGE REGISTER
332
80 COUNTER
INPUT OF COMPUTATION STATUS
333
ARITHMETIC SECTION
INPUT OF DATA TO BE PROCESSED
334
512-BIT DATA REGISTER GROUP
335
HEXADECIMAL COUNTER
COMPUTATION ENABLE SIGNAL
DATA SELECTION SIGNAL
CLOCK SIGNAL
ADDRESS SIGNAL
WRITE DATA SIGNAL [31:0]
WRITE STROBE SIGNAL

FIG. 32

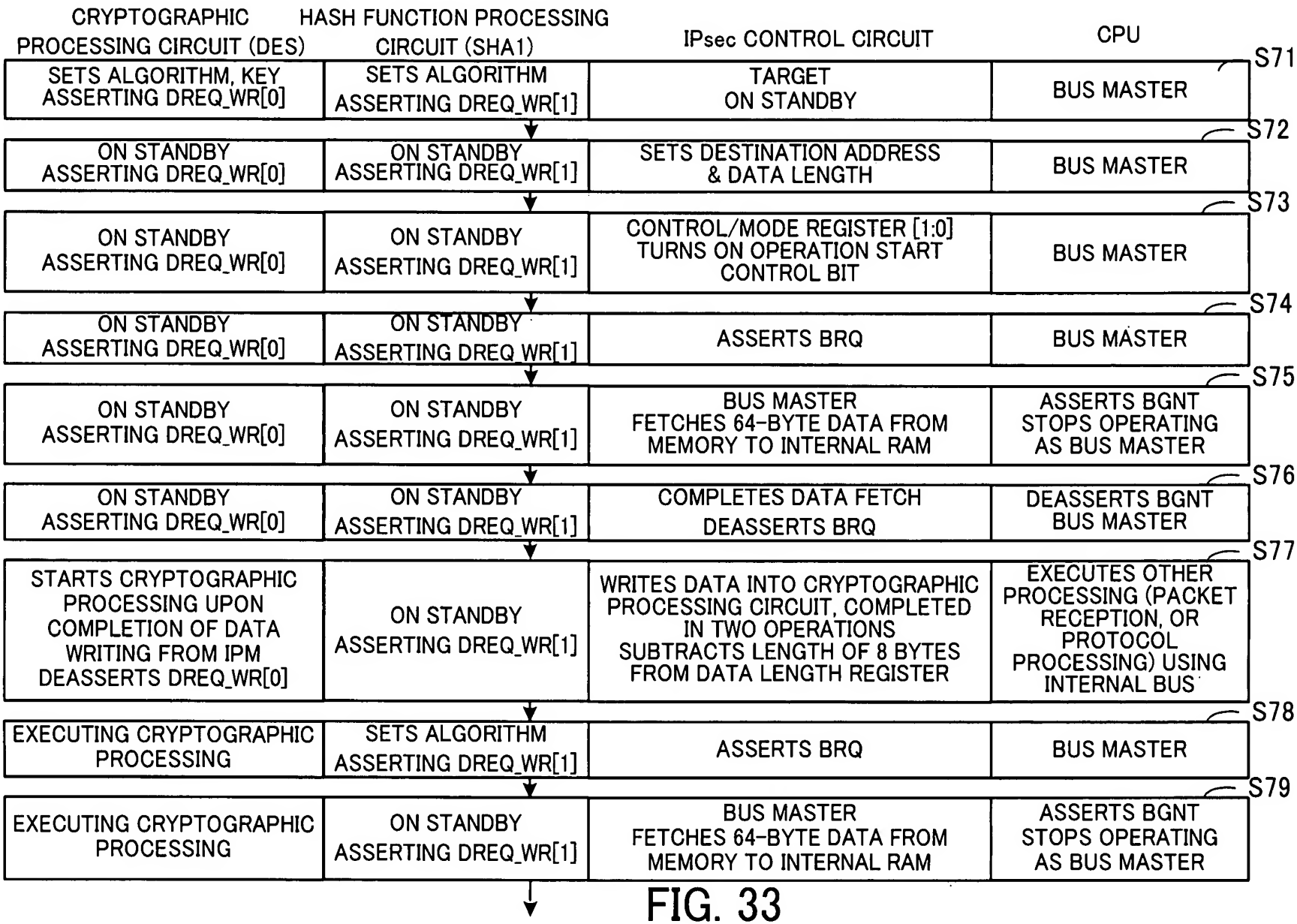


FIG. 33

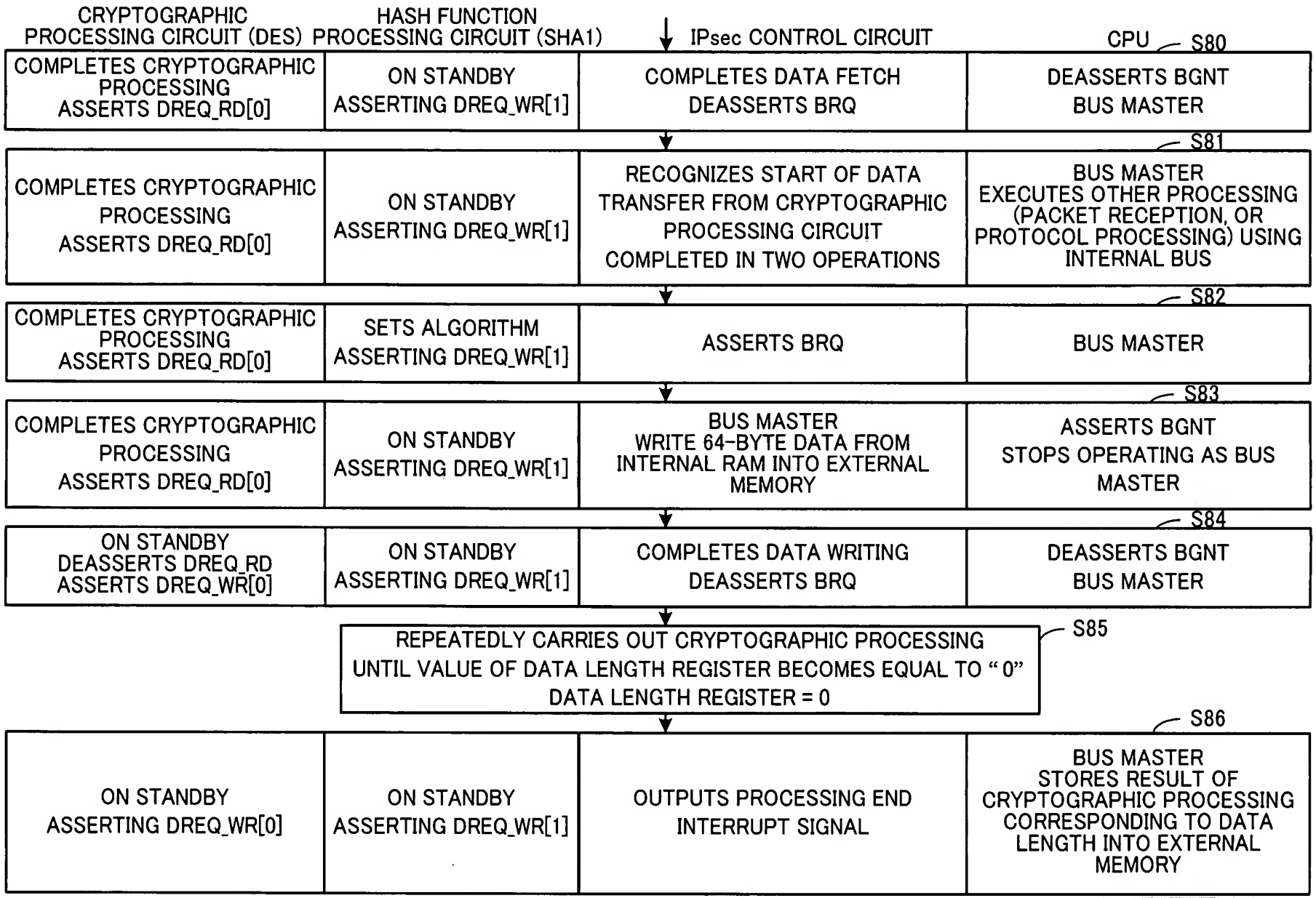


FIG. 34

Title: INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA SECURITY DEVICE
Inventor: Kenichi IIZUKA et al.
Docket Number: 108273-00006

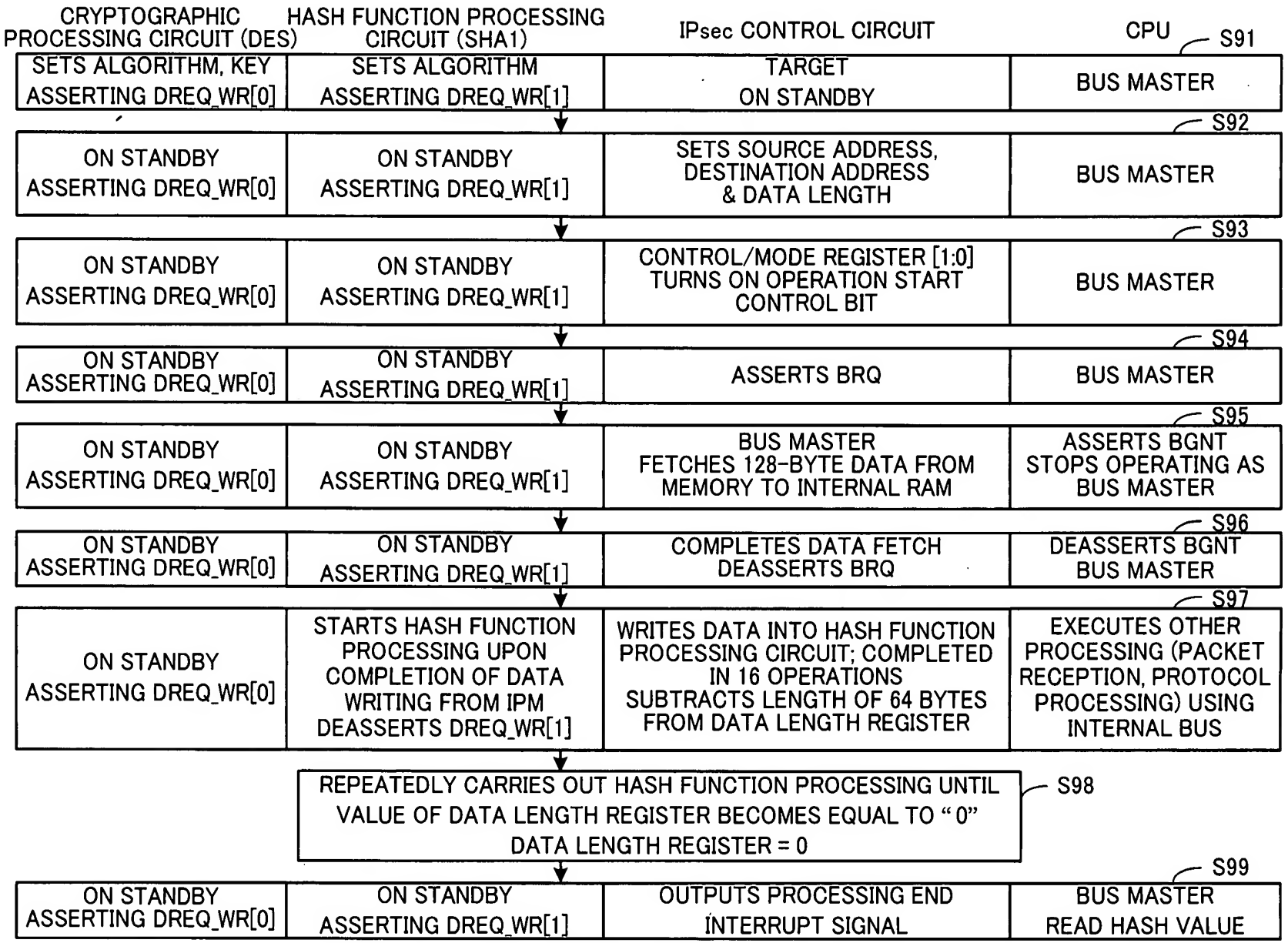


FIG. 35

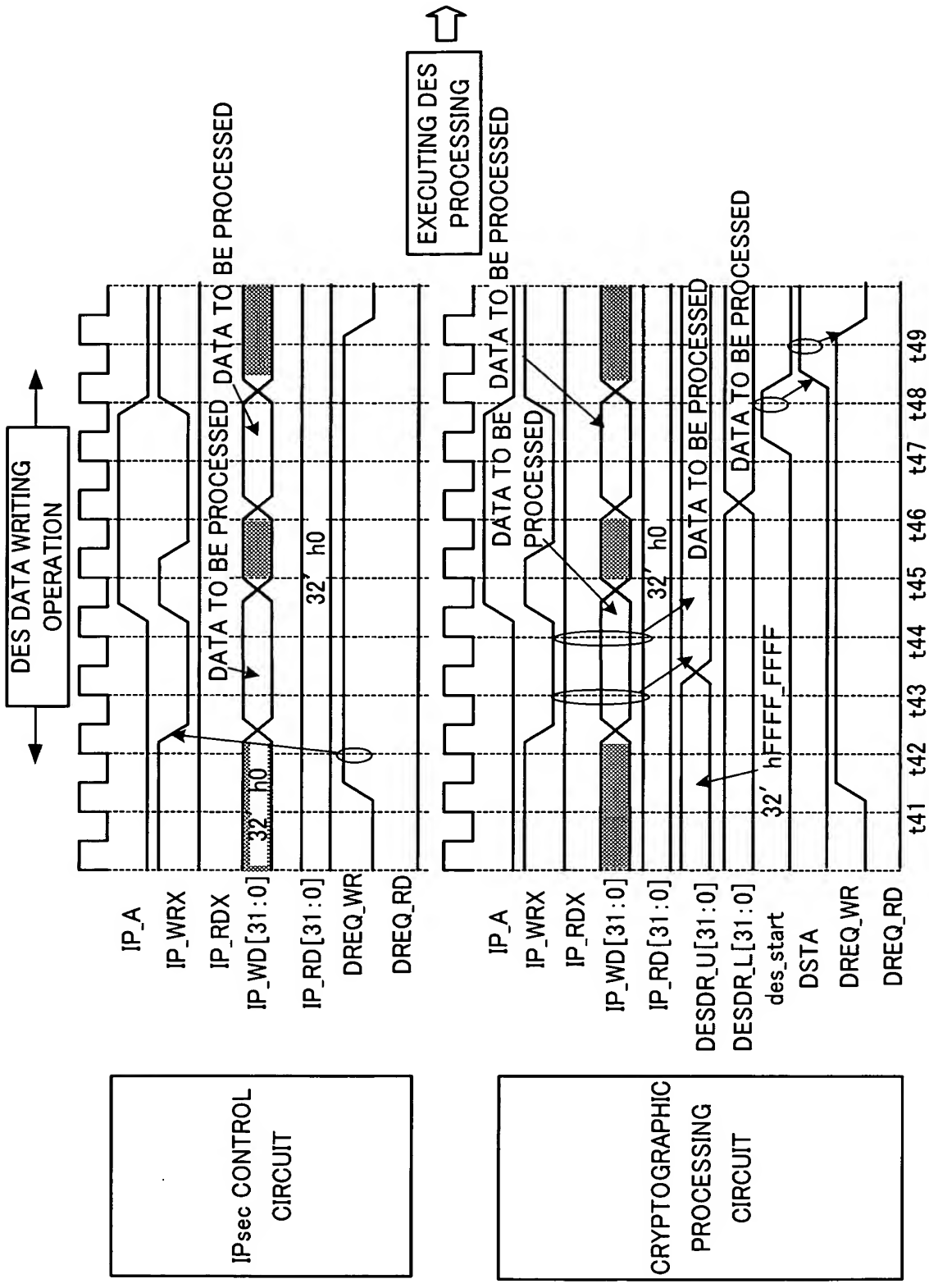

IPsec CONTROL CIRCUIT
CRYPTOGRAPHIC PROCESSING CIRCUIT
DES DATA WRITING OPERATION
EXECUTING DES PROCESSING
IP_A
IP_WRX
IP_RDX
IP_WD[31:0]
IP_RD[31:0]
DREQ_WR
DREQ_RD
DESDR_U[31:0]
DESDR_L[31:0]
des_start
DSTA
DATA TO BE PROCESSED
32' h0
32' hFFFF_FFFF
t41
t42
t43
t44
t45
t46
t47
t48
t49

FIG. 36

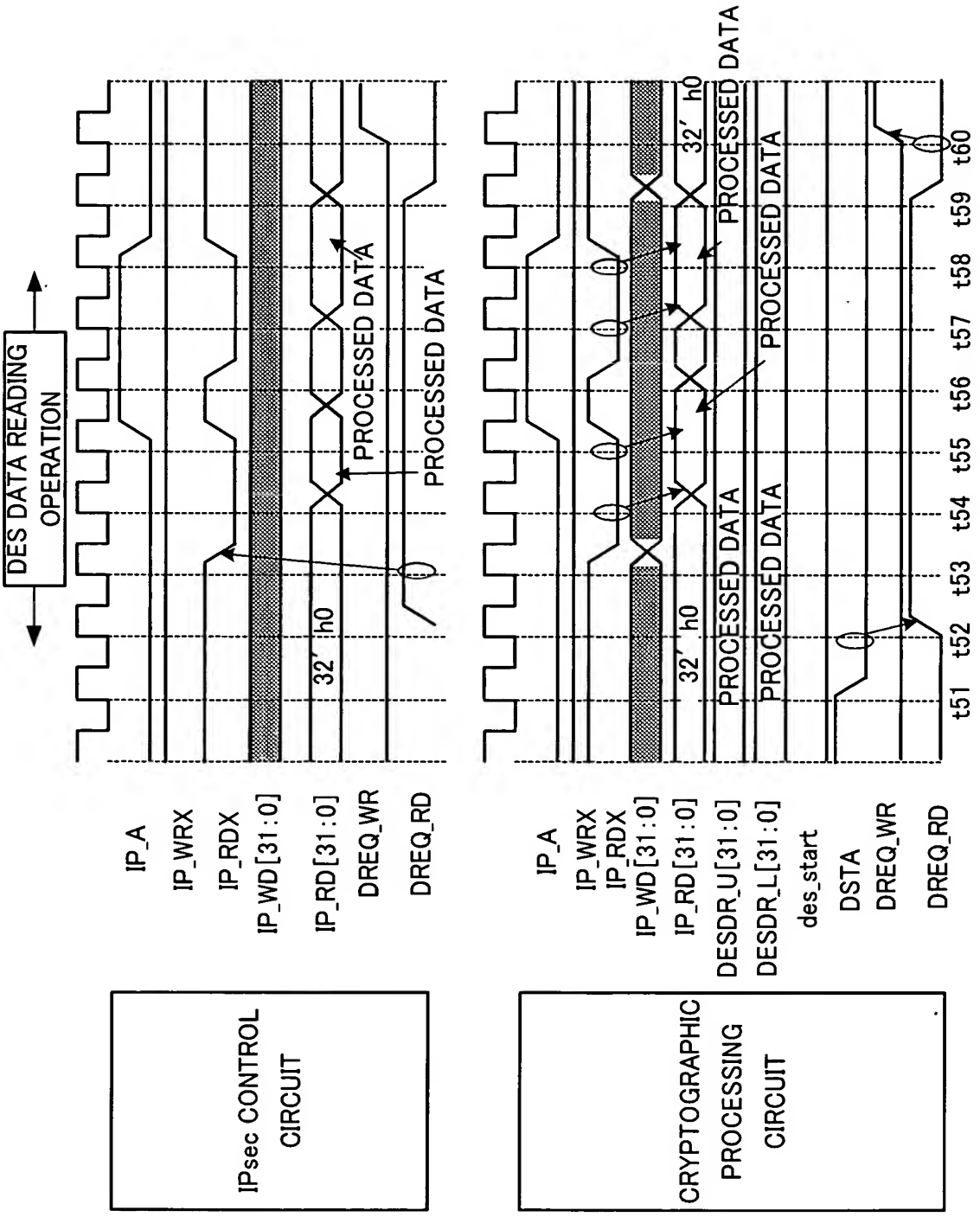

IPsec CONTROL CIRCUIT
IP_A
IP_WRX
IP_RDX
IP_WD[31:0]
IP_RD[31:0]
DREQ_WR
DREQ_RD
32'h0
PROCESSED DATA
PROCESSED DATA
DES DATA READING OPERATION
CRYPTOGRAPHIC PROCESSING CIRCUIT
IP_A
IP_WRX
IP_RDX
IP_WD[31:0]
IP_RD[31:0]
DESDR_U[31:0]
DESDR_L[31:0]
des_start
DSTA
DREQ_WR
DREQ_RD
32'h0
PROCESSED DATA
PROCESSED DATA
PROCESSED DATA
PROCESSED DATA
t51
t52
t53
t54
t55
t56
t57
t58
t59
t60

FIG. 37

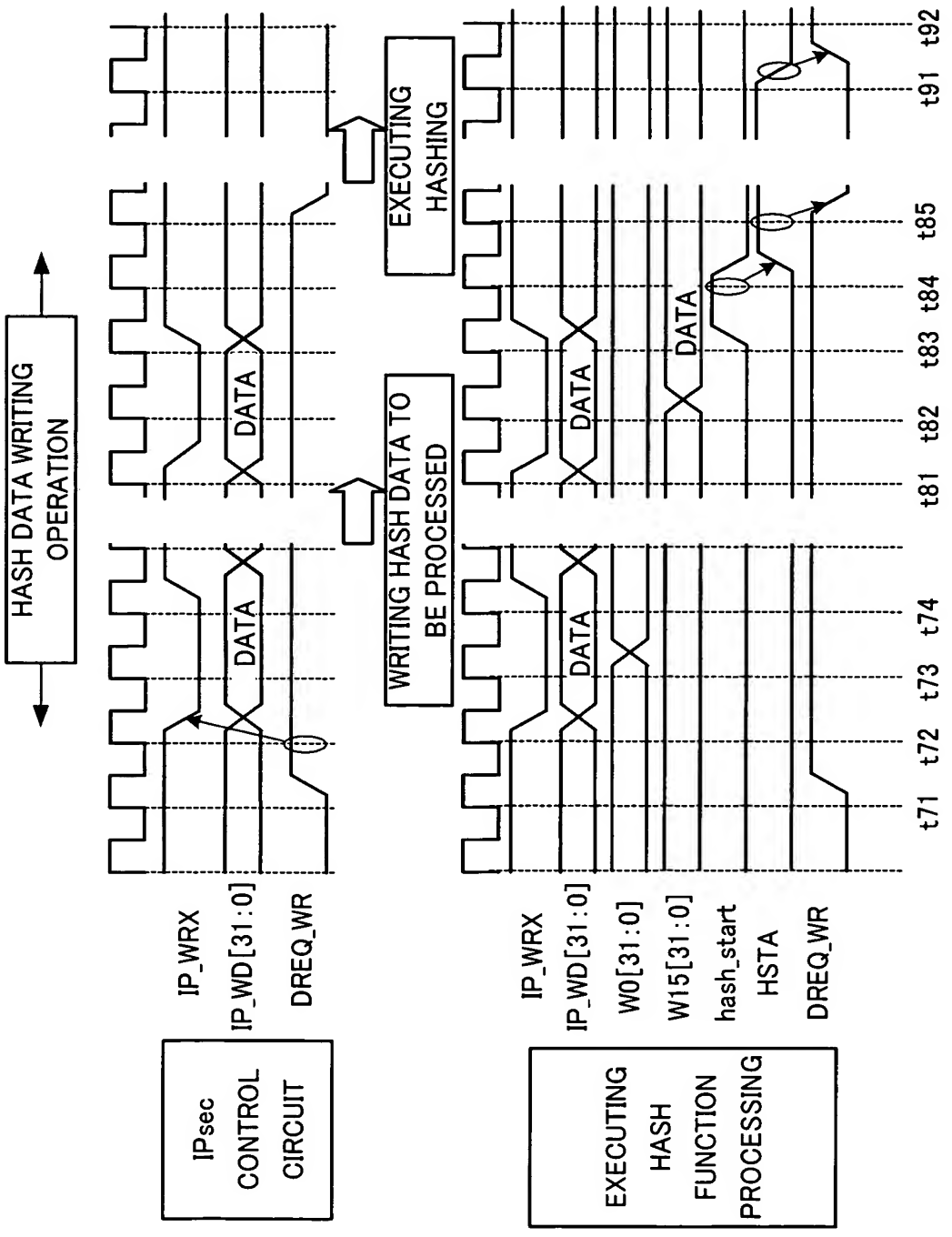

HASH DATA WRITING OPERATION
IPsec CONTROL CIRCUIT
IP_WRX
IP_WD[31:0]
DREQ_WR
DATA
WRITING HASH DATA TO BE PROCESSED
EXECUTING HASHING
EXECUTING HASH FUNCTION PROCESSING
IP_WRX
IP_WD[31:0]
W0[31:0]
W15[31:0]
hash_start
HSTA
DREQ_WR
DATA
t71 t72 t73 t74 t81 t82 t83 t84 t85 t91 t92

FIG. 38

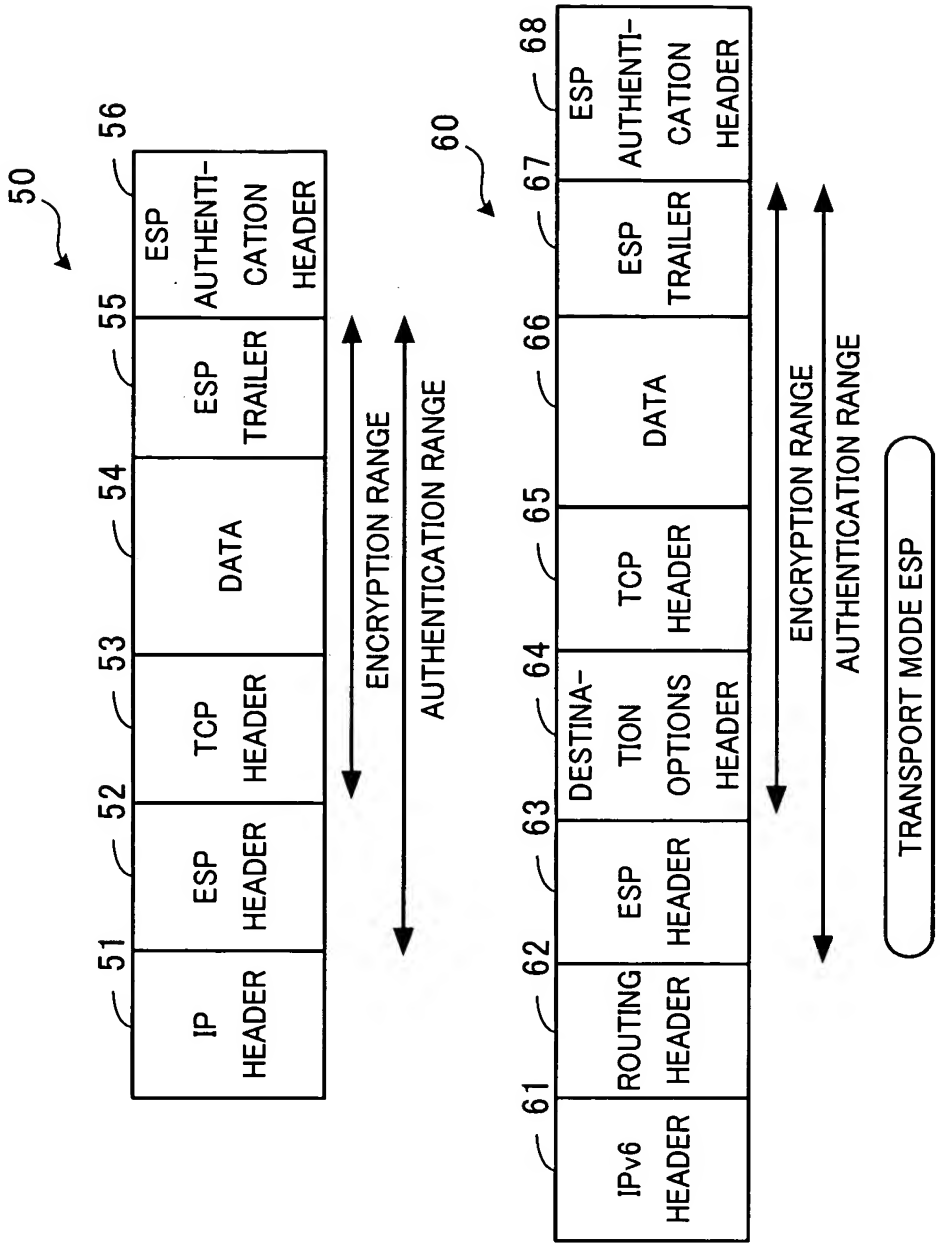


FIG.39A IPv4

FIG.39B IPv6

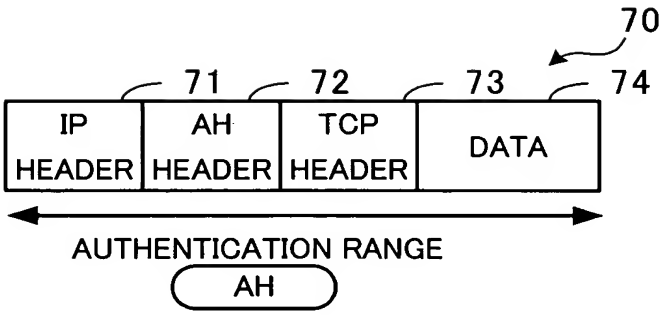
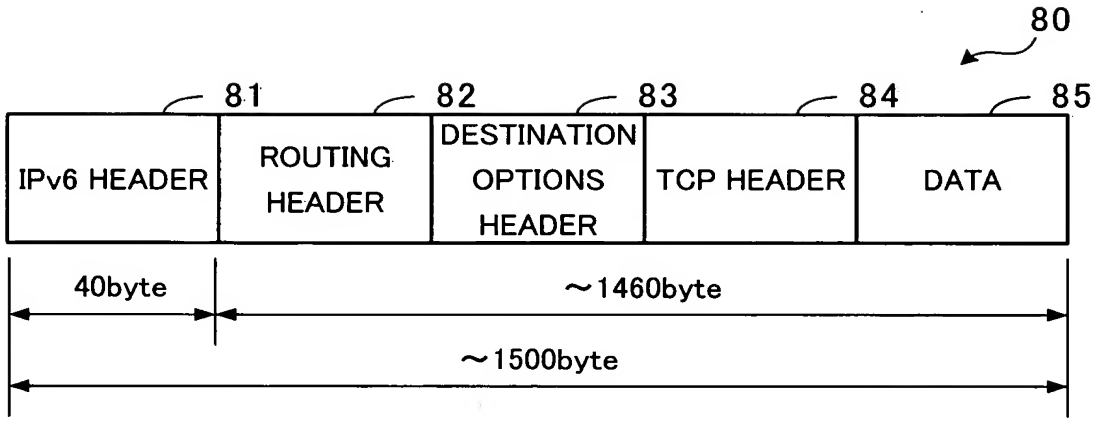

70
71
72
73
74
IP HEADER
AH HEADER
TCP HEADER
DATA
AUTHENTICATION RANGE
AH

FIG. 40



IP PACKET SIZE

FIG. 41

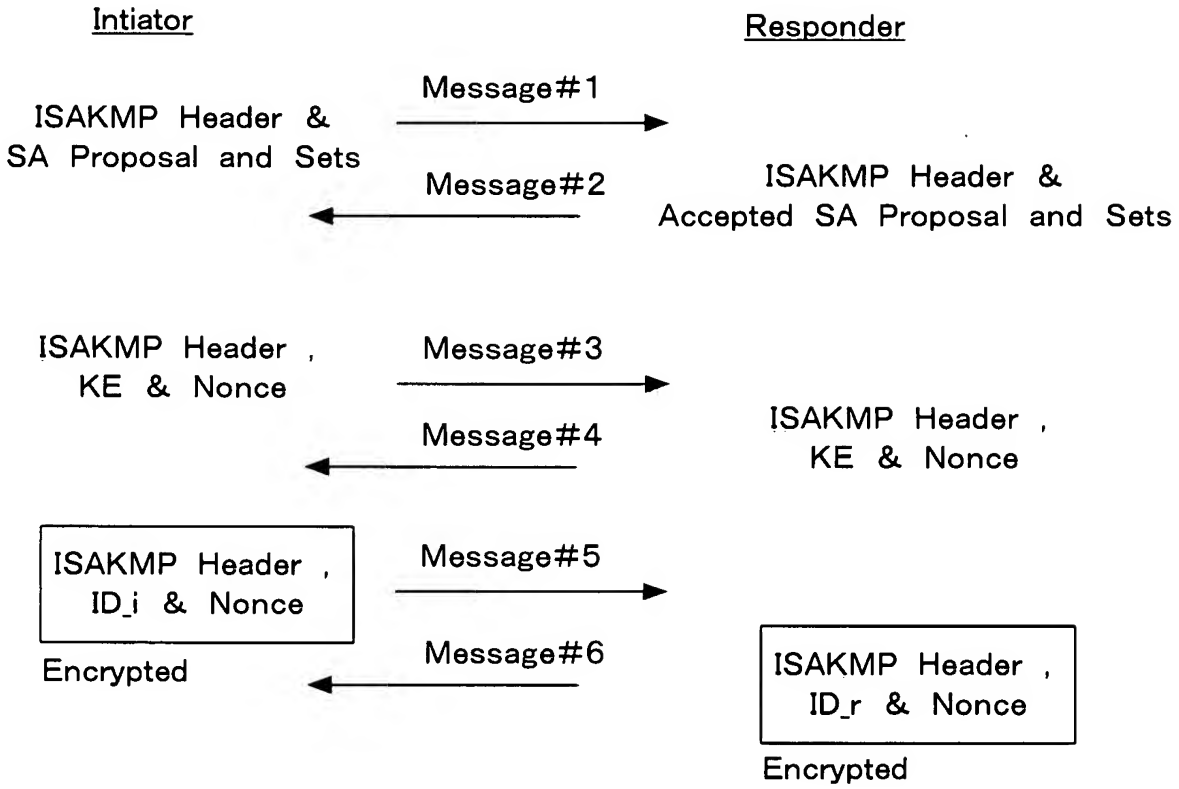


FIG. 42

3DES-CBC- CRYPTOGRAPHIC PROCESSING

1496-BYTE DATA PROCESSING PERFORMACE SPEED UNIT/ μs ec

	3DES-CBC-ENCRYPTION	3DES-CBC-DECRYPTION
SOFTWARE	264917	264919
CPU + CRYPTOGRAPHIC PROCESSING CIRCUIT	2977	2979
IPsec CONTROL CIRCUIT + CRYPTOGRAPHIC PROCESSING CIRCUIT	579	581

FIG. 43

HMAC-SHA1 HASH FUNCTION PROCESSING
1500-BYTE DATA PROCESSING PERFORMACE SPEED UNIT/ μsec

	HMAC—SHA1
SOFTWARE	41309
CPU + HASH FUNCTION PROCESSING CIRCUIT	2258
IPsec CONTROL CIRCUIT + HASH FUNCTION PROCESSING CIRCUIT	297

FIG. 44

Title: INTER-BUS COMMUNICATION INTERFACE DEVICE AND DATA SECURITY DEVICE
Inventor: Kenichi IIZUKA et al.
Docket Number: 108273-00006

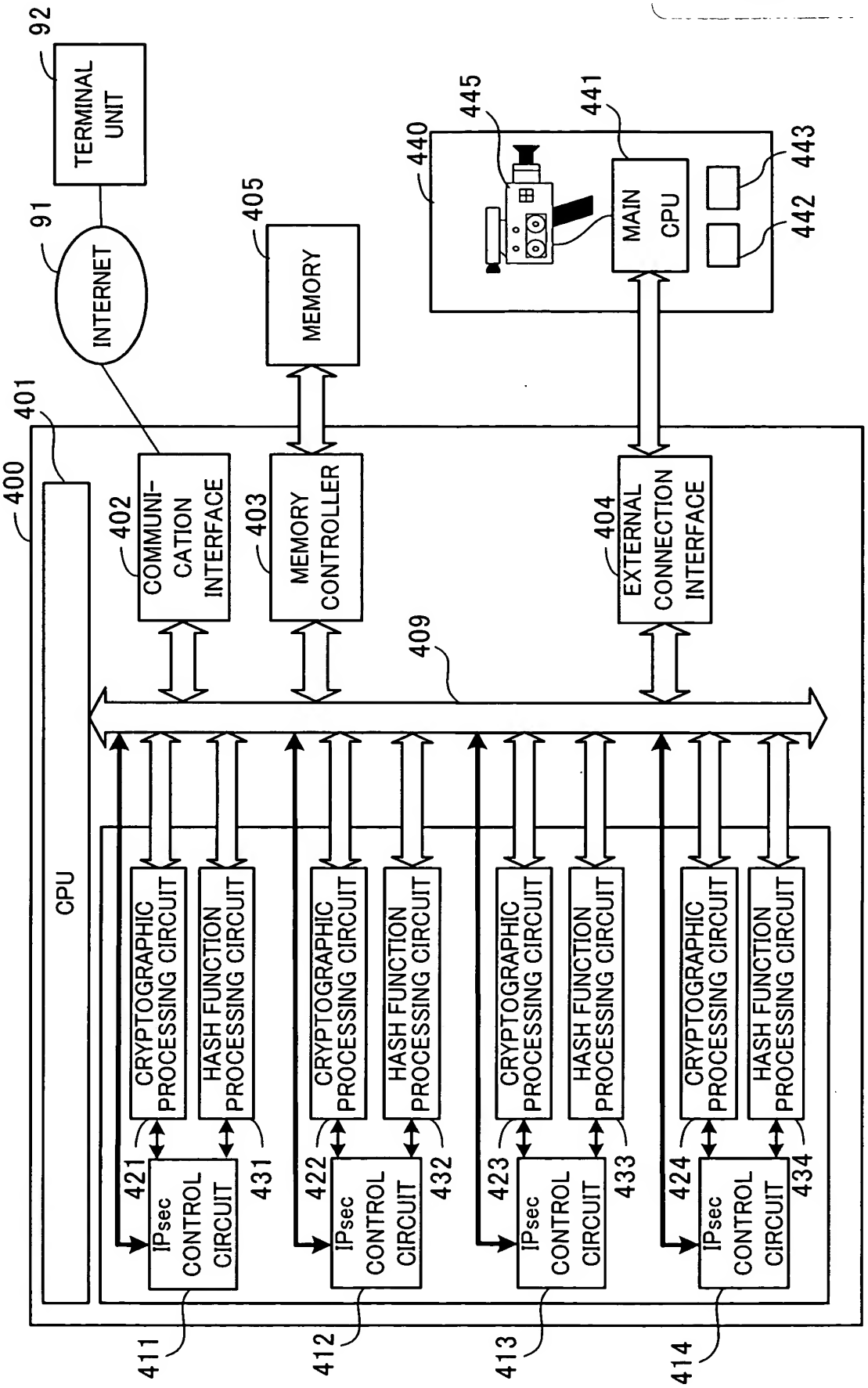


FIG. 45

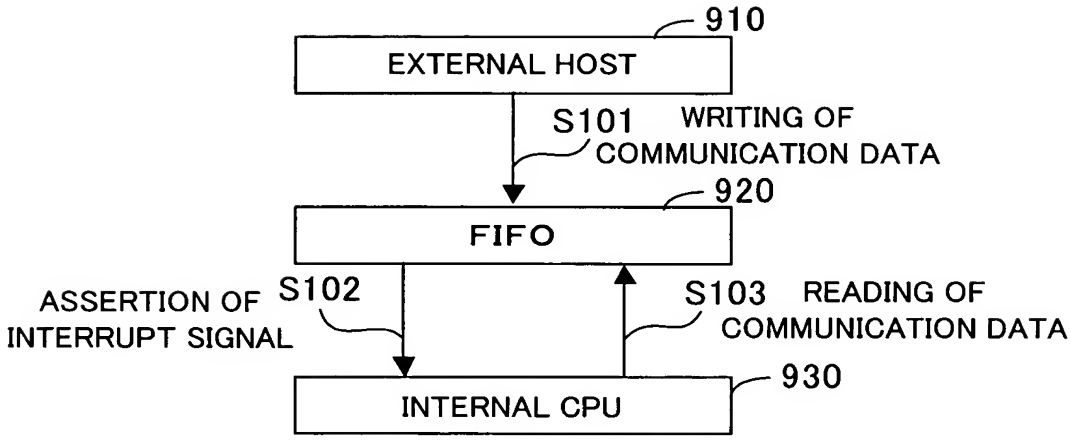

910
EXTERNAL HOST
S101
WRITING OF COMMUNICATION DATA
920
FIFO
ASSERTION OF INTERRUPT SIGNAL
S102
S103
READING OF COMMUNICATION DATA
930
INTERNAL CPU

FIG. 46

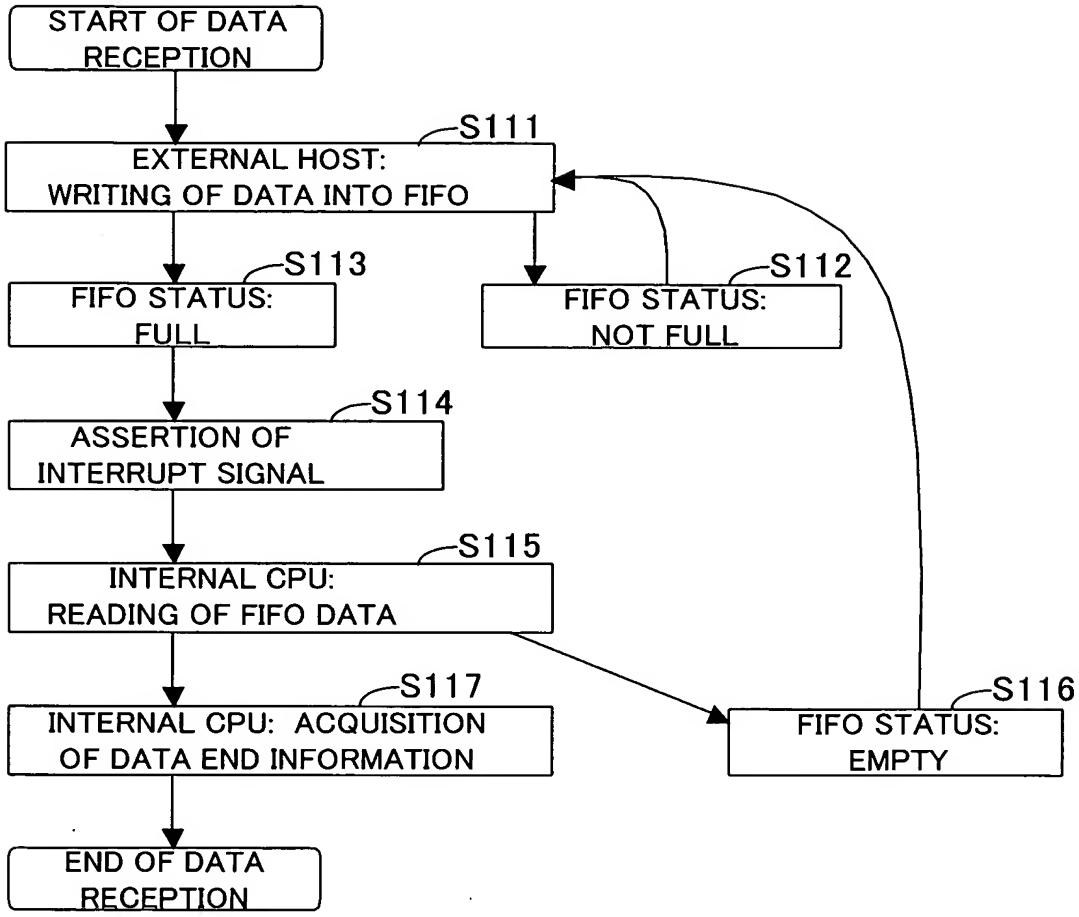

START OF DATA RECEPTION
S111
EXTERNAL HOST: WRITING OF DATA INTO FIFO
S113
FIFO STATUS: FULL
S112
FIFO STATUS: NOT FULL
S114
ASSERTION OF INTERRUPT SIGNAL
S115
INTERNAL CPU: READING OF FIFO DATA
S117
INTERNAL CPU: ACQUISITION OF DATA END INFORMATION
S116
FIFO STATUS: EMPTY
END OF DATA RECEPTION

FIG. 47

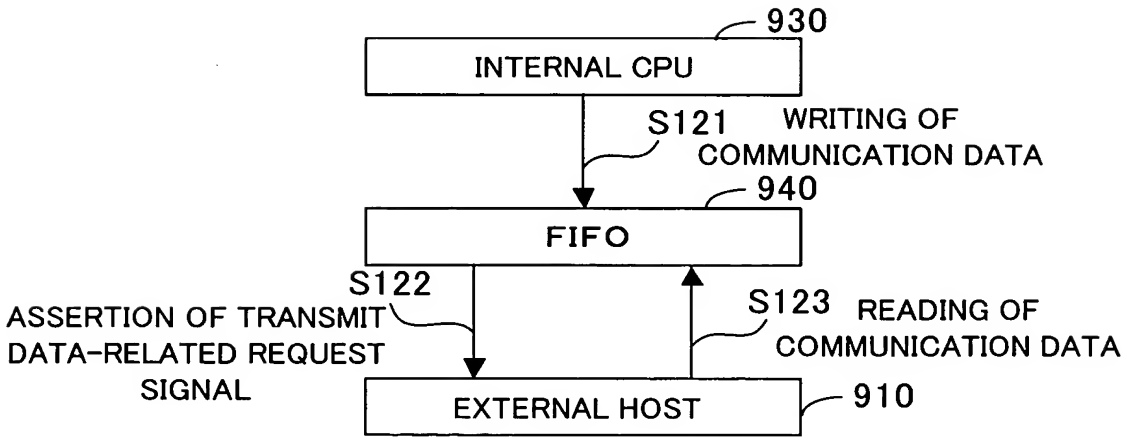

930
INTERNAL CPU
S121
WRITING OF COMMUNICATION DATA
940
FIFO
S122
ASSERTION OF TRANSMIT DATA-RELATED REQUEST SIGNAL
S123
READING OF COMMUNICATION DATA
EXTERNAL HOST
910

FIG. 48

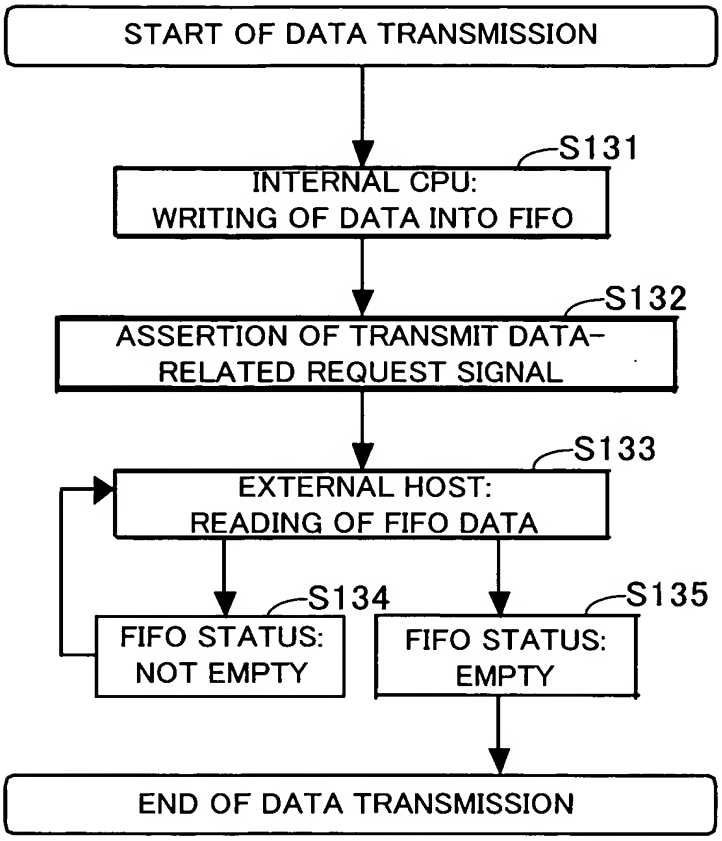

START OF DATA TRANSMISSION
S131
INTERNAL CPU:
WRITING OF DATA INTO FIFO
S132
ASSERTION OF TRANSMIT DATA-
RELATED REQUEST SIGNAL
S133
EXTERNAL HOST:
READING OF FIFO DATA
S134
FIFO STATUS:
NOT EMPTY
S135
FIFO STATUS:
EMPTY
END OF DATA TRANSMISSION

FIG. 49